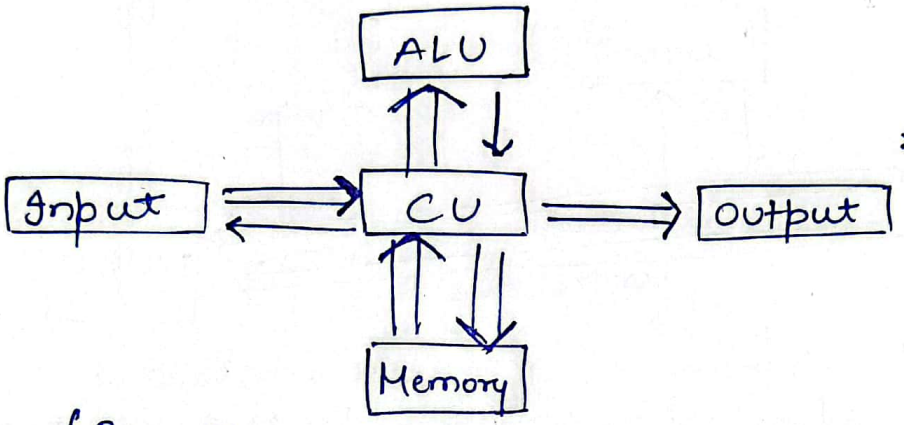
*Microprocessor:

Up is a clock driven programmable electronic device which accept binary data, process it according to the instruction stored in its memory. for its operation it requires register to hold data temporarily and permanently.



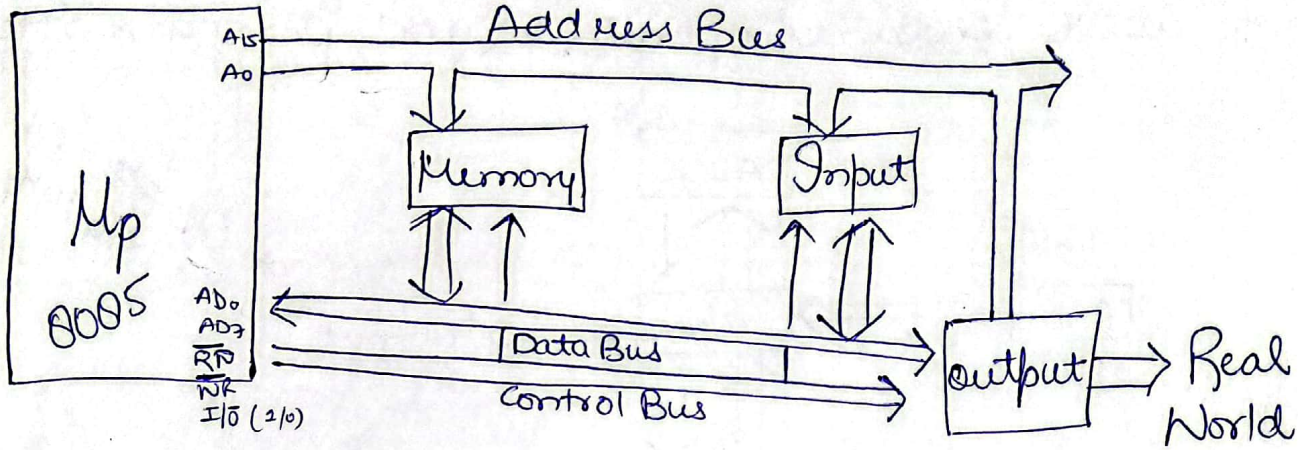
* 8237 = IC
* T = 1x10^-9 GHz

fig: Block diagram of Up.

- **Arithmatic and logic Unit:** It is responsible to perform arithmatic op. on binary data such as addition, subtraction, increament/decreament. and by successive addition or substraction it can perform multiplication and division. It also perform logical operations such as logical AND, OR, NOT, NOR, etc.
- **Input and Output devices:-**
- **Control Unit:** It is main part of microprocessor. It control all the operations of itself and other supporting devices like I/O and memory. It receives information from memory and after decoding it up generates control signals to other parts.
- **Memory:** It is an another imp. part of Up Unit. In this, it has RAM and ROM both memory. ROM memory is used to store interrupts inst, Interfacing device port number and some address for periferal devices.

RAM memory is required to stored data during ALU operations & programmable inst.

#Bus Structure of Microprocessor:

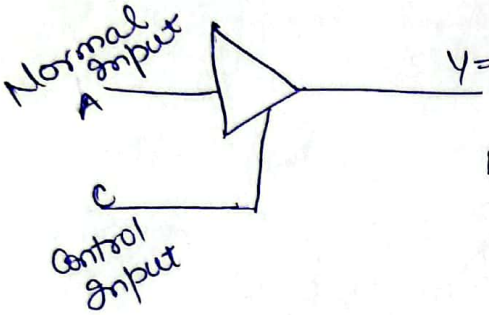


- **Address Bus:** A D Bus is a unidirectional group of 16 signal line which carry 16 bit memory address or 8 bit ~~bit~~ I/O device port address. The address Bus is used to identify peripheral or memory location.
- **Data Bus:** D B is bidirectional group of 8 lines which transfer data b/w mp memory and peripheral devices. 8085 Mp has 8 bit data Bus by this Mp can handle ~~to~~ $2^8 = 256$ or ranging from 00H to FFH no. of data.
- **Control Bus:** C B consist Various individual control lines which perform the specific task in AB or DB all lines work simultaneously but in control Bus each signals perform a special operation like Memory select, I/O select, Read, Write, Bus Ideal Operation.

#logic Devices for Interfacing:

Several types of Interfacing devices are necessary to interconnect the components of Bus oriented system. The logic devices are tri-state Buffer, Bus drivers units → Uni-directional, Bi-directional, Decoder, Encoder.

- **Tri-State Buffer:** A tristate is a digital ckt that shows three stages two stages are normal ON and OFF (0 and 1) as the Credential logic gates and the third stage high Impedence this stage behaves as open Ckt between IO, in this state change in I/p does not ~~affer~~ effect Output.

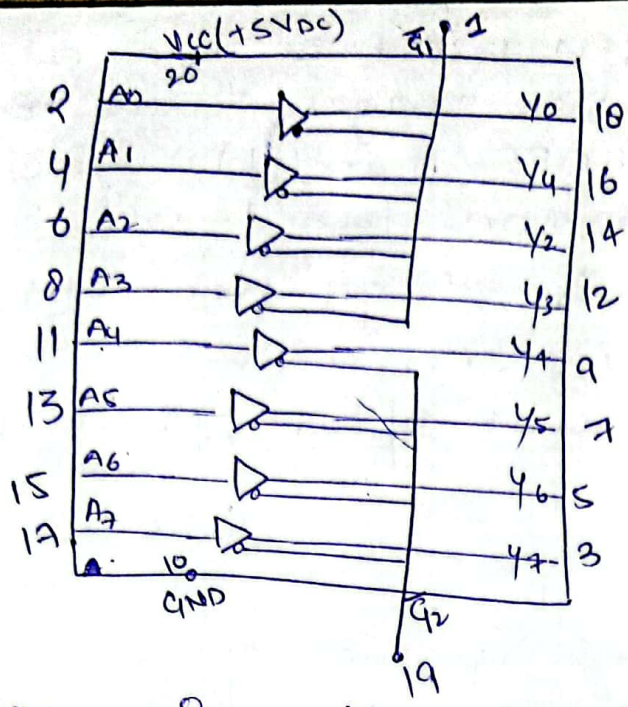


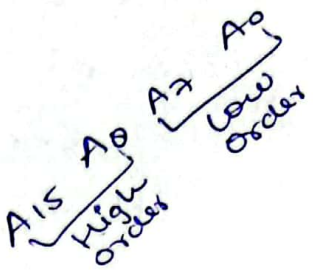
- **Bus Driver Buffer:**

Bus Driver Buffer are used to increase driving Capacity of Buses. Mp system has two types of Bus: unidirectional or Bidirectional. To drive these buses we have two types of Buffers: Unidirectional Buffer and Bidirectional Buff

- **Unidirectional Buffer:**

Address Bus is unidirectional bus. To drive address bus we use IC 74LS244 as a unidirectional buffer as shown in figure. It consist 8 input and 8 output lines and each line consist with tristate buffer i.e, divide 8 to two groups G_1 and G_2 controlled by two control signals. When $\overline{G_1}$ and $\overline{G_2}$ connected to +5VDc (logic 1) the data is tranfer from Input to Output as normal Wire. But when $\overline{G_1}$ and $\overline{G_2}$ connected to GND it enters in tri-state logic (high Impedence).

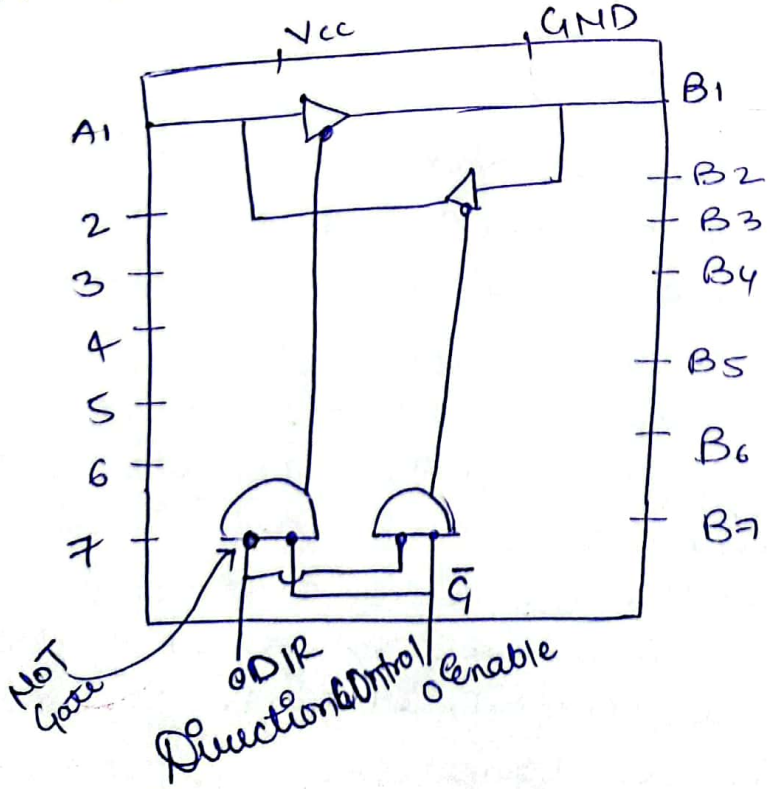




In this situation, thus transfer o/p is remain unchanged but it disconnect to Input. This 74LS244 is used to drive high order address Bus.

Bidirectional Buffer:

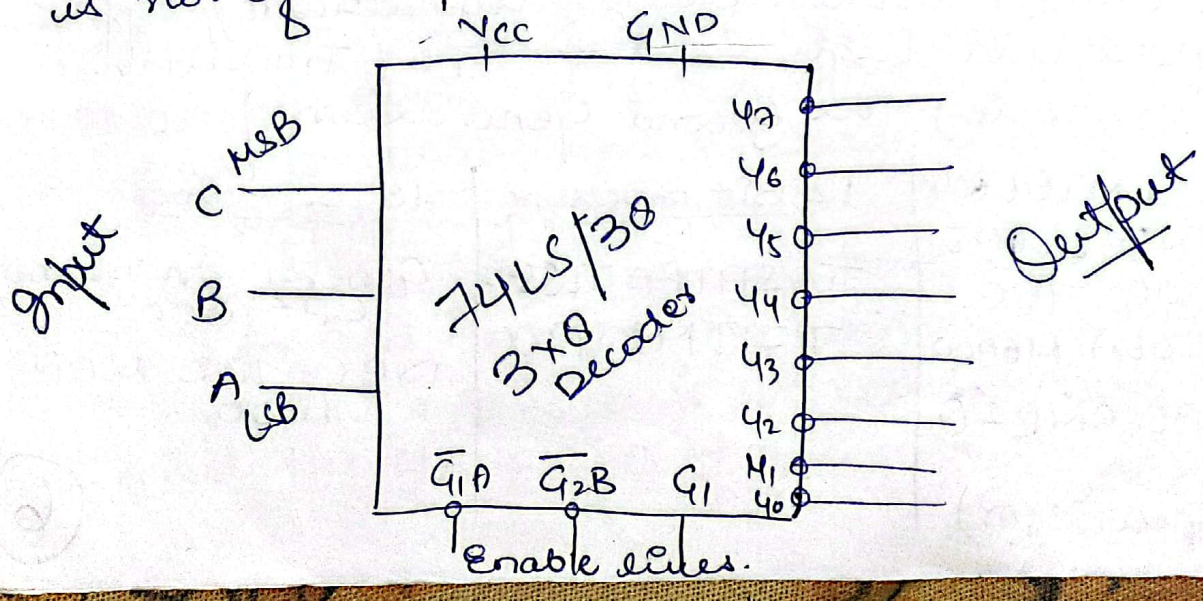
Bidirectional Buffer is used to drive data Bus it is also c/d optal Bus Transreceiver Its IC No. is 74ALC45



It consist 16 non-inverting buffer. Each input has 2 buffers with opposite direction buffer. connection so 8 buffer work for one direction. The direction of data flow control by DIR (Direction pin) when signal on this pin is high the data transfer from left to right side and when it is of level the direction of data flow is opposite. Direction and enabling the buffers is controlled by an ANDed op. of direction signal and gate signal. Its controlling op. is show by functional Table

$\bar{G}$	DIR	operation
L	L	Right to left
L	H	left to Right
H	X	Isolation / Impedance / tri-state

- **Decoder:** It is a logic ckt that identify each combination of signal present at input and provide output at one output signal corresponding to input. The relation b/w input & output $2^m = n$ where n is no. of input and m is no. of output.



74LS/38 decode is a 3x8 decoder it is used in mp system. to decode the address line to identify memory loc. 2 decoders are used to identify 16 bit memory add. It has 3 ip and 8 active low output. It has 3 enable input. The enable input are $\bar{G}_2B$ and $\bar{G}_1A$ are connected to GND. G_1 is connected logic 1 &. The decoder is enable and it gives output with corresponding input.

#Evolution of Microprocessor:

▲Intel Coorperation USA introduce first mp intel 4004 to the real world in 1971. It is 4 bit Microprocessor and it can handle and access 4096 memory loc. with 4 bit data storage Capacity. It can support 45 Inst. and this is fabricated by PMOS technology with large scale Integration (LSI) so this is known as first Generation of Mp. (1971-1973)

1971
Other Mp of this generation are INTEL 4004, INTEL 4040, FAIR CHILD PPS.25, NATIONAL IMP-4, ROCHWELL PPP-4 (4 bit processor)

1973
Other Mp of this generation are INTEL 8008, AMI 7200, ROCKWELL PPS-8. (4 bit processor)

▲In later, 1973 the NMOS technology the one used for manufacture of Mp technology offers fastspeed and high density TTL (Transistor Transistor logic) The Second Generation processor are

	12 bit processor	16 bit processor
INTEL 8080	TOSHIBA TLCS-12	General Instrument CP-1600
INTEL 8085	TI TMS 9900	DEC-WD MCP-1600
ZILOG Z80		
MOTOROLA M6800		
NATIONAL CMP-8		
(8 bit processor)		

The second generation were *40pin ICs, large memory space handeling capacity, fast Op. and better interrupt handeling capacity.

▲ In 1970, the third generation of Mp were introduced. There are 16 bit processor. and used HMOS technology. This generation processor are 40/48/64 pins processors. The size of internal registor are 0/16/32 bit and it can access 1-16 MegaByte memory Third Generation having high handling capability and flexible Input/Output port addressing. Mp of third Generation are.

INTEL 8086/80000/80286
MOTOROLA 68000/68010
ZILOG Z8000

- **Encoder:**

Encoder is the digital combination ckt that provide a coded form output of each input. If more than one input are active or enable at a time simultaneously than encoder gives wrong coded form of input. It cannot be identify the both to remove this problem we select priority encoder.

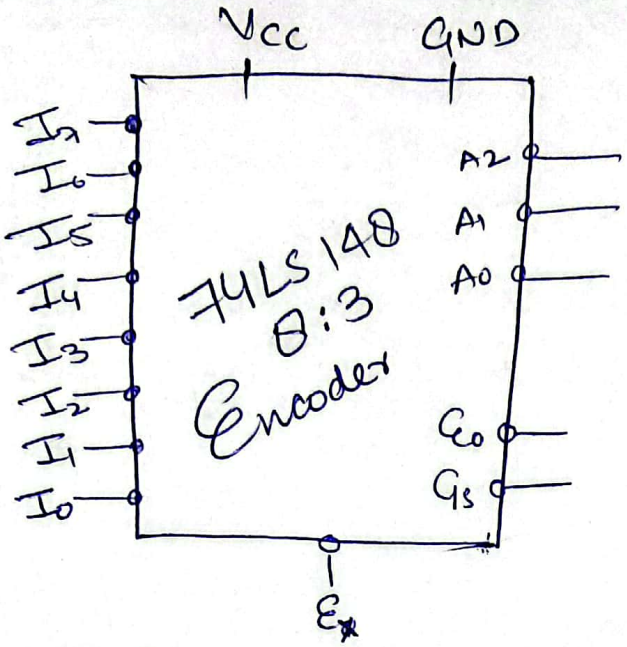
- **Priority Encoder (IC-74LS140):**

It is a 8x3 encoder in this all 8 inputs have priority according to there values higher value has highest priority and Encoder select one input according to high to low priority.

→ The 8 inputs are normal priority inputs from I_0 to I_7 and A_0 to A_2 are normal outputs.

→ The Enable signal E is connected to ground to start the operation of Encoder.

(X)



→ The signal Eo and Gs are use in cascading op. When more than one coder are used to work on 16 data inputs.

→ Encoder is used to control 16 Bit address Bus of microprocessor.

▲ Fourth Generation were introduced in 1980. It is 32 bit processor with low power version using HMOS are fabricated with a strong instruction set. The processor are INTEL 80386, INTEL 80486, MOTOROLA M68030.

▲ Fifth Generation, after 1980 the INTEL Coorperation has taken a leading role in Up company. In 1982 the pertium series were launched as considered as fifth generation. PENTIUM - I/ Pro/ II/ III/ IV

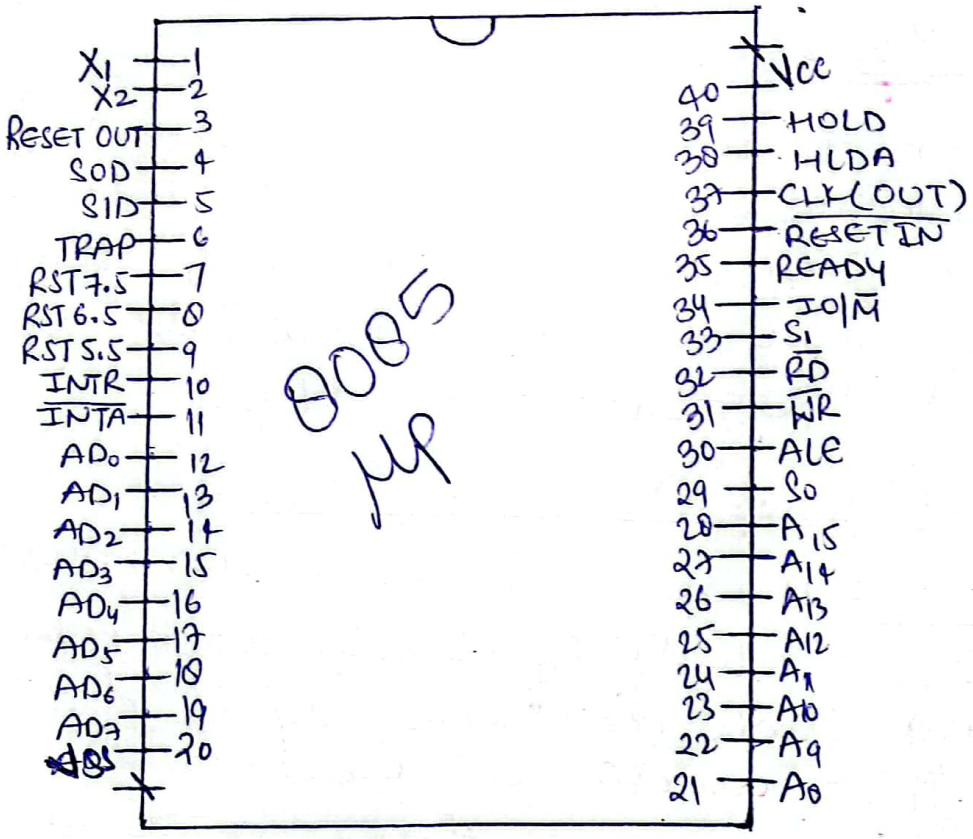
#8085 Up:

INTEL Coorperation introduce 8085 Up in late 1973. It is a second gen. up. It has following features -

Features of 8085:

(1) It is 8 bit µp. It can accept, process and provide 8 bit data simultaneously.
(2) It operates at +5 volt DC supply connected on it's Vcc pin.
(3) It operates with 5MHz clock frequency.
(4) It has 16 bit address Bus. It can access $2^{16} = 2^6 \times 2^{10} = 64K$ memory location of 8 bit data storage capacity each.
(5) It can access $2^8 = 256$ No. of I/O ports.
(6) It provide interrupt facility by 5 hardware interrupts pin.

- 8085 µp is a 40 pin DIP (Dual Inline Package) IC.



All the 40 pins are classified into 7 groups acc to the func performing by them which are-

1) Power supply & frequency signals.
2) Address & Data Bus
3) Control Signals (Bus)
4) Interrupt signals
5) Serial Input / Output Signals
6) DMA signal
7) Reset signal.

Power Supply & Frequency signal:

- **Vcc :-**
  At Vcc pin we provide +5V DC supply
- **Vss :-**
  This pin is connected to ground all logic 0.
- **X_1 & X_2 :-**
  Between these two pin a crystal oscillator is connected which generate 10MHz frequency signal. The oscillator ckt half the generated frequency signal & provide internal clock frequency of 5MHz.

Data Bus & Address Bus:

- **$AD_0 - AD_7$:** These 8 bit data bus multiplexed with lower half of 16 bit address bus during each machine cycle for first time state T_1 it works as lower order address Bus & remaining time state of machine cycle it works as Bi-directional Data Bus.

- **$A_0 - A_{15}$:**
The higher Byte of memory address is loaded on these 8 bit Bus. After first time state of each m/c cycle is goes in High Impedence logic or tri-state logic.

Control & status signal :
IO/$\overline{M}$, S_0, S_1 each group of signal indicates the nature of operation which is to be performed by µp

- **ALE (Address Latch Enable) :**
ALE signals responsible for distributing the memory address into two part :-
A_{15} - A_0 higher Byte and A_7 - A_0 lower Byte.

- **$\overline{RD}$ and $\overline{WR}$ pin :-**
These two control signal active low signal which control the data ^received from memory or Input device or ^data send to memory or O device.

- **Ready :-**
This pin is used by periferal or interfacing devices to check the µp is ready for op. or not.

Interrupt Signals :
8085 µp have five hardware interrupt pin. TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR.
If all the interrupts activate at a time then µp identify them acc. to their priorities. TRAP has highest priority and INTR has lowest ^or least priority.

After the end of current inst execution.

#Serial I/O Signal:

SID pin is use to accept data serially bit by bit from external device. SOD pin is serial output data at this pin Microprocessor send out or transmit data serially bit by bit to external device.

#DMA Signal:

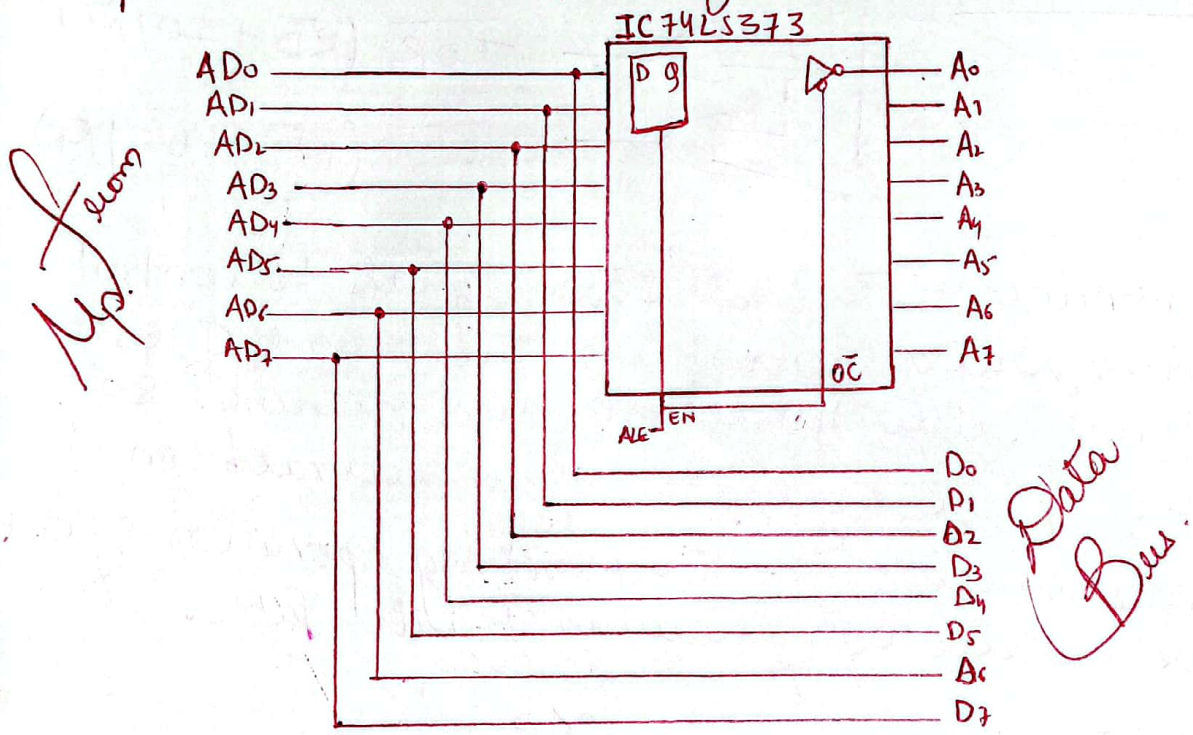
HOLD and HLDA are DMA signal. The HOLD signal indicate up that another device requesting for used of address bus, control Bus & data Bus. HLDA pin hold acknowledgement pin at this pin up send a signal to DMA and release their control on address Bus, data Bus & control Bus.

#RESET Signals:

- **RESET IN:** This is active low signal pin when up receives signal on this pin. up perform following operations -
  (1) set PC at 0000H memory address.
  (2) Reset all the interrupts & HOLD Acknowledgement flip-flop.
  (3) Tri-state the data, address and control Bus
- **RESET OUT:** This pin is used by up to reset the other periferal devices to initialize a synchronized clock signal pulse.
- **INTR:** At this pin up send active low signal to indicate the peripheral device in the reference of INTR.
- **CLK OUT:** At this pin up send synchronize clock signal to the interfacing device or ~~the~~ peripheral device to synchronize their op. with itself.

Demultiplexing of $AD_0 - AD_7$:

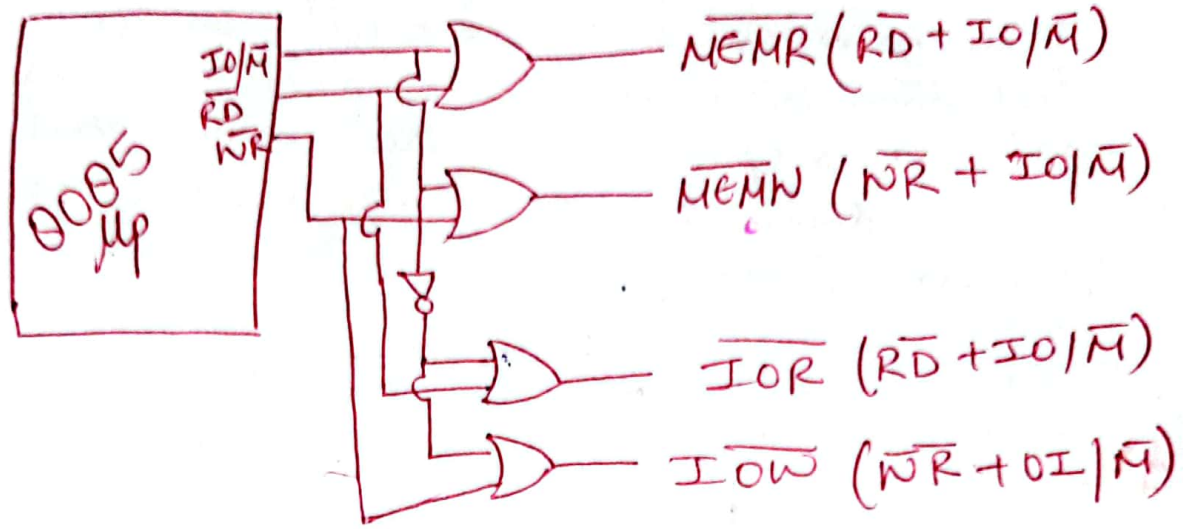
The data bus is multiplexed with lower address Bus to reduce the no. of pins in Up chip bcz the m/p address is identify at the beginning of each machine cycle and remaining time these lines are in tri-state logic so to utilize data lines efficiently with multiplexed with lower order address bus and data bus. Demultiplexing process is done by ALE signal the ckt shown in fig.



IC74LS373 is a 8 bit latch having 8 Flip-flop at each i/p line at the starting of m/c cycle. (Time T_1) Up activate ALE signal which enable the latch and data available on the I/p side $AD_0 - AD_7$ Consider as lower byte of m/p address at the time state T_2 ALE disable which enable tri-state buffer control signal ($\overline{OC}$) and remaining time of m/c cycle it works as tri-state logic and I/p input available on $AD_0 - AD_7$ lines considered as data Bus. Thus the demultiplexing is

perform and this process is repeated on beginning of each m/c cycle.

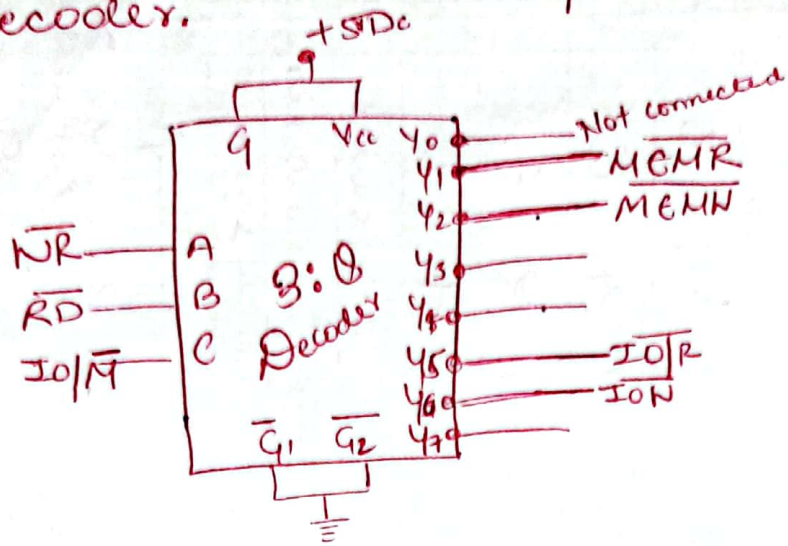
Generation of Control Signals:



8085 µp provide IOR and IOW signal to control read and write operation. The read & write op. performs with I/O device and memory. So OI/M̄, RD̄, or WR̄ generate four separate control signal as shown in fig. The working operation of ckt can be realize by following truth Table.

I/P			O/P			
I/O/M̄	RD̄	WR̄	MEMR̄	MEMW̄	IOR̄	IOW̄
0	0	0	Condition never exist bez RD̄ and WR̄ never active simultaneously.			
0	0	1	0	1	1	1
0	1	0	1	0	1	1
0	1	1	1	1	1	1
1	0	0	RD̄ & WR̄ Never active at a time			
1	0	1	1	1	0	1
1	1	0	1	1	1	0
1	1	1	1	1	1	1

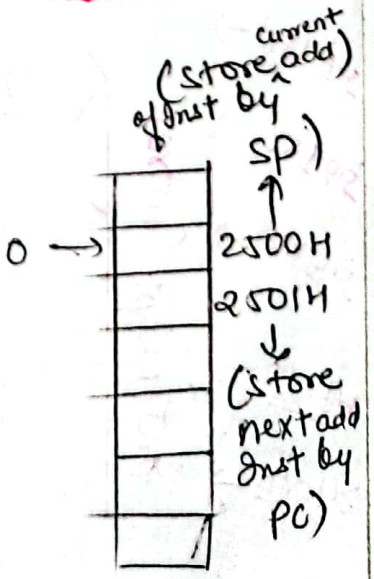
The truth table can be implemented by using 3:8 Decoder.

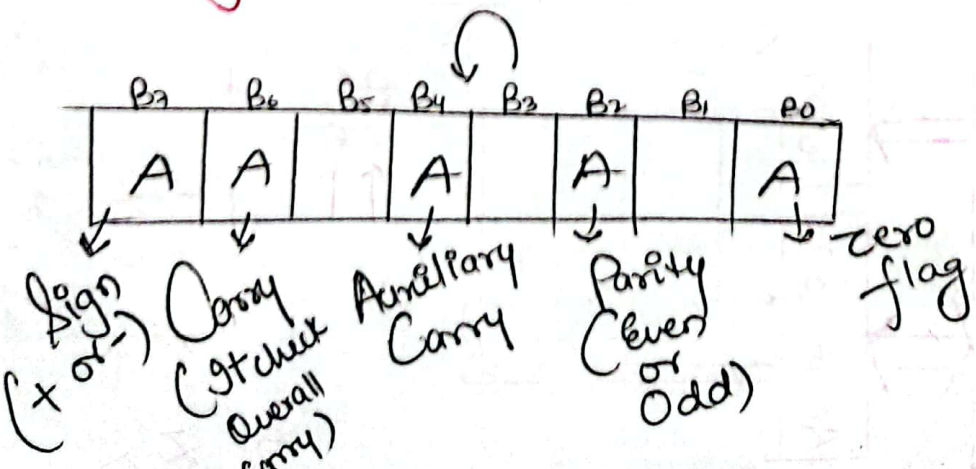


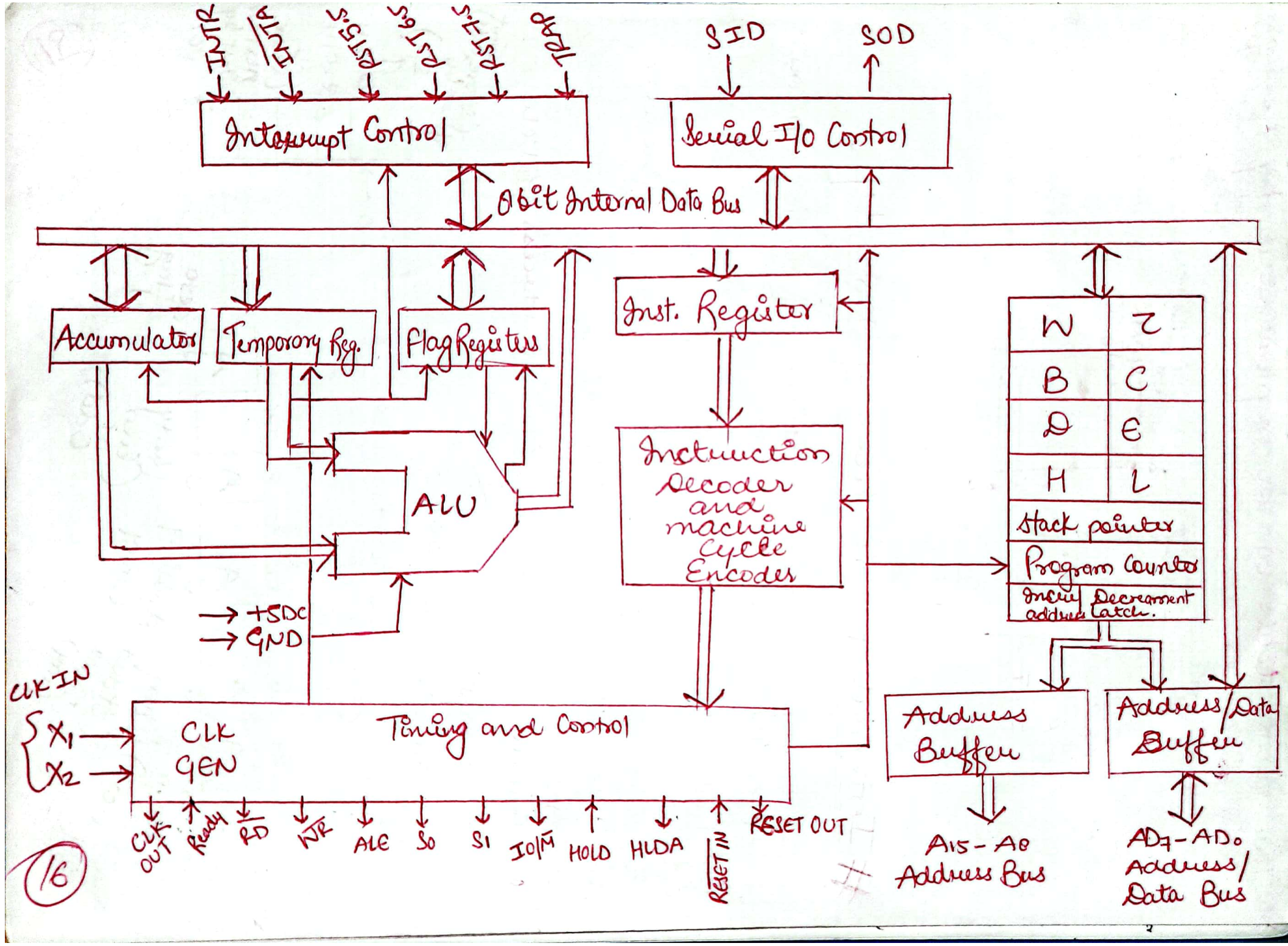
#Internal Architecture of 8085 Up

The internal architecture of 8085 Up consist following functional blocks.

(1) Registers
(2) ALU
(3) Instruction Decoder & machine cycle Encoder
(4) Address Buffer
(5) Address / Data Buffer
(6) Increament / Decreament address latch
(7) Interrupt Control
(8) Serial I/O Control
(9) Timing and control Ckt.






INTR
INTA
RST5.5
RST6.5
RST7.5
TRAP
SID
SOD
Interrupt Control
Serial I/O Control
8 bit Internal Data Bus
Accumulator
Temporary Reg.
Flag Registers
ALU
Inst. Register
Instruction Decoder and machine Cycle Encoder
W
Z
B
C
D
E
H
L
Stack pointer
Program Counter
Increment address Latch.
Decrement
+5DC
GND
CLK IN
X1
X2
CLK GEN
Timing and Control
Address Buffer
Address/Data Buffer
CLK OUT
Ready
RD
WR
ALE
S0
S1
IO/M
HOLD
HLDA
RESET IN
RESET OUT
A15 - A8
Address Bus
AD7 - AD0
Address/ Data Bus

Register : 8085 has 8 addressable 8-bit registers A, B, C, D, E, H, L and two 16 bit register PC and SP. These registers are classified in four groups -

• General purpose Register :

B, C, D, E, H, L are six General purpose register. These can be used separately to store 8 bit data and B pair C, D pair E and H pair with L to store 16 bit data. H, L pair register pair also functions as a m/m pointer for initializing each m/c cycle in default case and in jump inst.

• Temporary Register :

The temporary registers are used by ALU for storing data to Arithmatic & logical op. W and Z registers are used to store 8 bit data during the execution of some special inst. Programmer cannot use these registers, 8085 used these register for their internal operation.

• Special Register :

Accumulator (A), flag register, Inst register are special registers. Accumulator is a 8 bit reg. It is used in arithmatic, logic, load & store op. as well as with Input Output related Operation. In default case after Arithmatic & logic op. the result is stored in Accumulator.

• flag Register :

It is a 8 bit register which indicate the

status of result after ALU related op. It has Five bactive flip flops.

- **Instruction Register:**

In every op. the up first fetch opcode of Inst from m/m & this opcode is stored in Inst reg.

- **16-bit Register:**

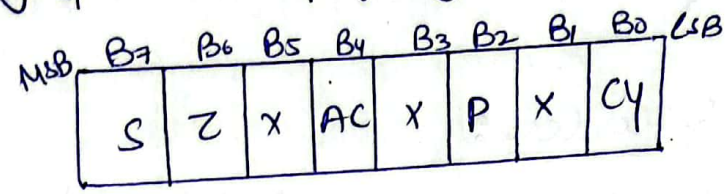
P.C and sp are 16-bit registers. Program is a sequence of Inst & up fetches these Inst. from m/m & executes them sequentially. The PC is a 16 bit register which store the ~~Inst~~ address of next Inst which is to be fetch. So it act as a pointer for next Inst. SP is a 16 bit register and stack is a reserve area of m/m in RAM and temporary Info. may be stored & SP hold the 16 bit address of the stack (initial m/m add. of portion of m/m) and it is used to hold address of last Inst. that had fetch recently.

W	Z
A	Flag Register
B	C
D	E
H	L
Stack Pointer	
Program Counter	

fig: Register Organization of 8085

Flag Register:

It is 8bit register in which 5 bits carries significant information in the form of flags which are sign flag (S), zero flag (Z), Auxiliary carry flag (AC), parity flag (P), Carry flag (CY) is shown in fig.



(1) Sign flag:

After the execution of Arithmatic or logical op. if bit '7' of the result is 1, the sign flag is set which indicate the result is negative. If bit '7' is 0, the ~~sign flag~~ result considered as +ve and flip flop is reset.

(2) Zero flag:

If the result after the A & L op. in ALU is zero then zero flag is set (Z=1) otherwise it is reset (Z=0)

(3) Auxiliary Carry flag:

In A or L op. there is a carry transfer to lower level to upper level (3rd bit to 4th bit) then AC flag is set to 1 otherwise it is reset 0.

(4) parity flag:

parity is defined by the no. of ones present in the result of Accumulator. If the result has even no. of ones the parity flag is set (P=1) if no. is odd parity flag is reset (P=0)

(5) Carry flag:

If there is a carry overflow out of bit 7 the carry flag set to 1 otherwise it is reset.

- **Instruction Register:**
In every op. of up, it fetch opcode of inst that opcode from its mm, that opcode is stored in inst register it is used to transfer the opcode to timing & control unit in synchronized way.

- **Instruction Decoder:**
Inst decoder receives the opcode of inst. and after decoding it provide the info. about the operation to timing and control unit.

- **Address Buffer:**
It is 8 bit unidirectional Buffer used to drive higher order Address Bus (A_{15}-A_8). It also use to tristate high order
RESET, HOLD, HLDA, HLT when address lines are not used.

- **Address/Data Buffer:**
It is 8 bit bidirectional buffer used to drive multiplexed address/Data Bus during first time state of each m/c cycle it drive lower order address Bus (A_7-A_0) as a address Bus as remaining time state (T-state) of m/c cycle it drive this Bus as data Bus. Under certain conditions RESET, HOLD, HLT, HLDA other certain conditions like Tristate it Tstate multiplex address Bus when it is not include.

- **Increament/Decreament address latch:**
It is a 16 bit reg. used to Inc/Dec the content of PC and SP 1 bit as a part of execution of inst. related to them.

Interrupt Control Unit:

Normal execution of program sometimes interrupt request are generated or received thus the program control transfer to program control Unit by temporary HALT. Main program and interrupt subroutine program is execute a/c to their priority of interrupt & after complete ~~comp~~ execution of subroutine of the program control shift to main program so the shifting of program control is governed by PCU.

Serial I/O control:

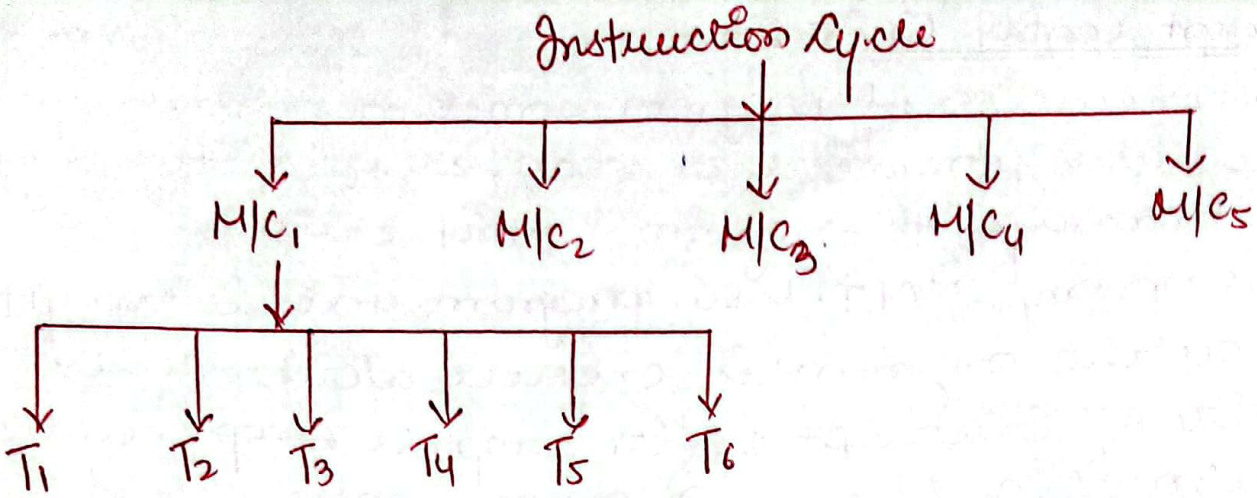
During the transmission of data over long distance, it is difficult to maintain parallel data Bus so serial Comm. is required. Serial I/O Unit transfer the control over data Bus at enable serial I/O pins. for bit by bit data transmission.

Timing and Control Unit:

The TPCU is main control centre of Up system It Control all op. of Up acc. to the info receive by Inst. decoder by generating synchronized signal with the help of Clock signal

Timing and Signals:

During the normal op Up fetch, decode and execute one Inst. after another inst. sequentially until HLT Inst. is executed. For fetching, decoding & execution of a single Inst constitute an inst cycle which consist 1-5 read or write op. b/w processor and m/m or b/w processor and IO device Each op. requires a particular time period i.e c/a m/c cycle and m/c cycle consist 3-6 time state (clock signal). Therefore, we can say one inst. cycle consist of 1-5 m/c cycle and one m/c cycle consist 3-6 time states.



There are 7 different types of m/c cycles in 8085 µp. The three status signals S_0, S_1 and IO/$\overline{M}$ identify each types of m/c cycle. Each signal are generated at beginning of each m/c cycle and remain valid for entire duration of cycle.

M/C cycle	Status signal			Control Signal		
	IO/$\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
1. Opcode fetch	0	1	1	0	1	1
2. Memory Read	0	1	0	0	1	1
3. Memory Write	0	0	1	1	0	1
4. I/O Read	1	1	0	0	1	1
5. I/O Write	1	0	1	1	0	1
6. INTA	1	1	1	1	1	0
7. Bus IDEL	0	0	0	1	1	1

✱Representation of signals:

µp synchronized its op. with clk signal in timing diagram. The whole operation is depend on clk freq signal.

Control Signal:

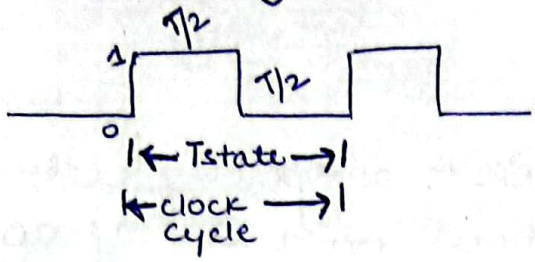


fig: Ideal clock signal

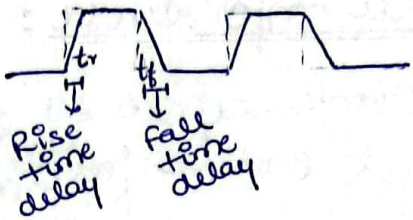
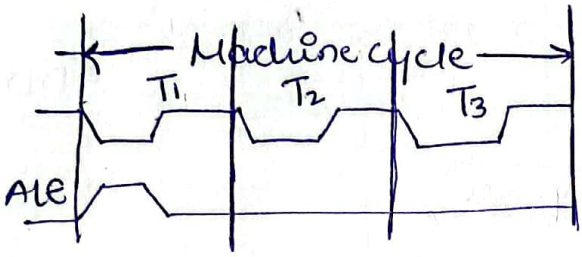


fig: Practice clock signal

Ideally clock should be square wave with rise and fall time but in practice we get rise and fall time therefore clock and other related signal are always shown with finite rise & fall time as shown in fig.

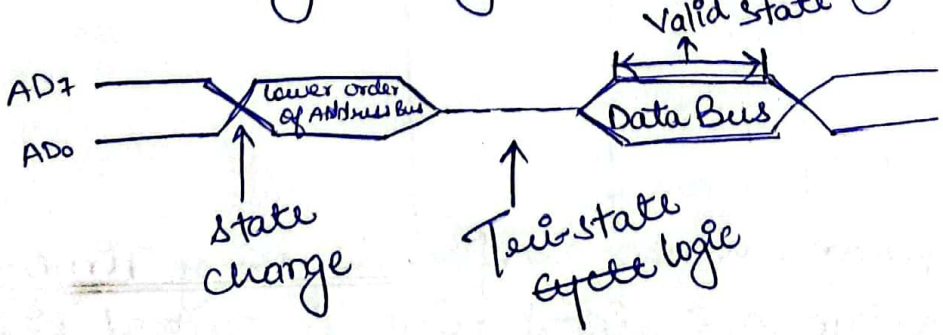
ALE:



At the beginning of each m/c cycle Mp enable ALE signal at instant of time and remaining time of M/c it is disable.

Group of signals:

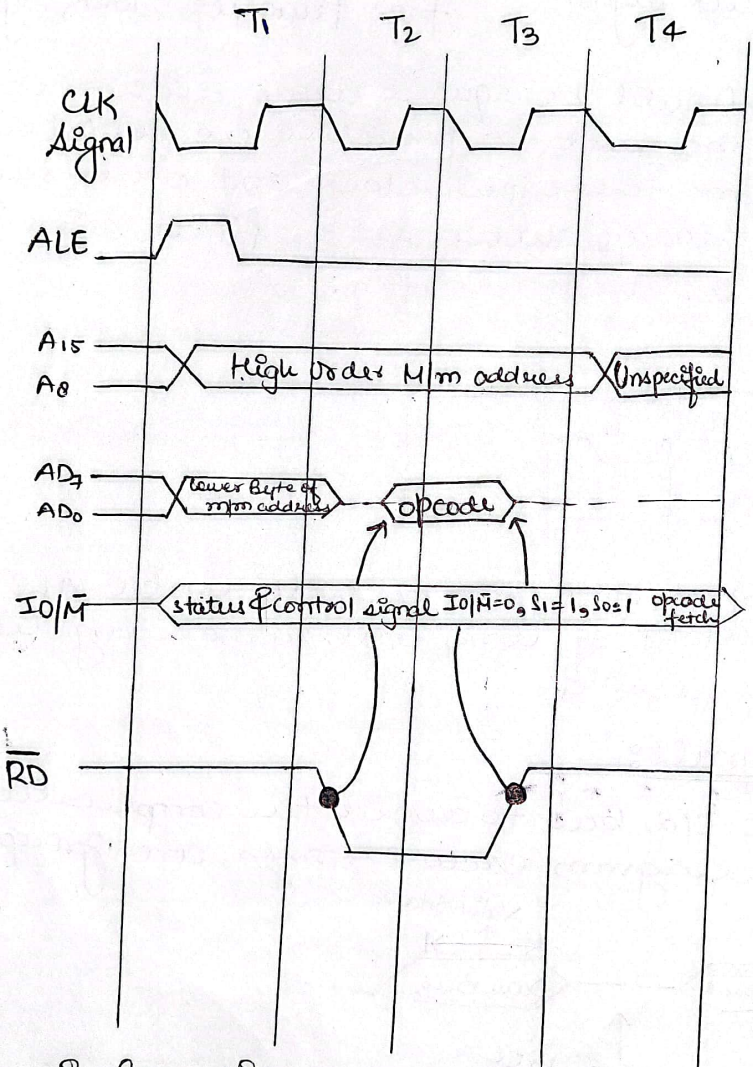
GOS are also c/d bus to avoid the complication in timing diagram each signals are group.



Timing Diagram:

Opcode fetch m/c cycle:

The first m/c cycle of every inst. is opcode fetch in this we get the info. along about nature of op.



ADD A, B

The timing diagram shown in fig. During Time State T1 → µp enable ALE signal upto instant of time.

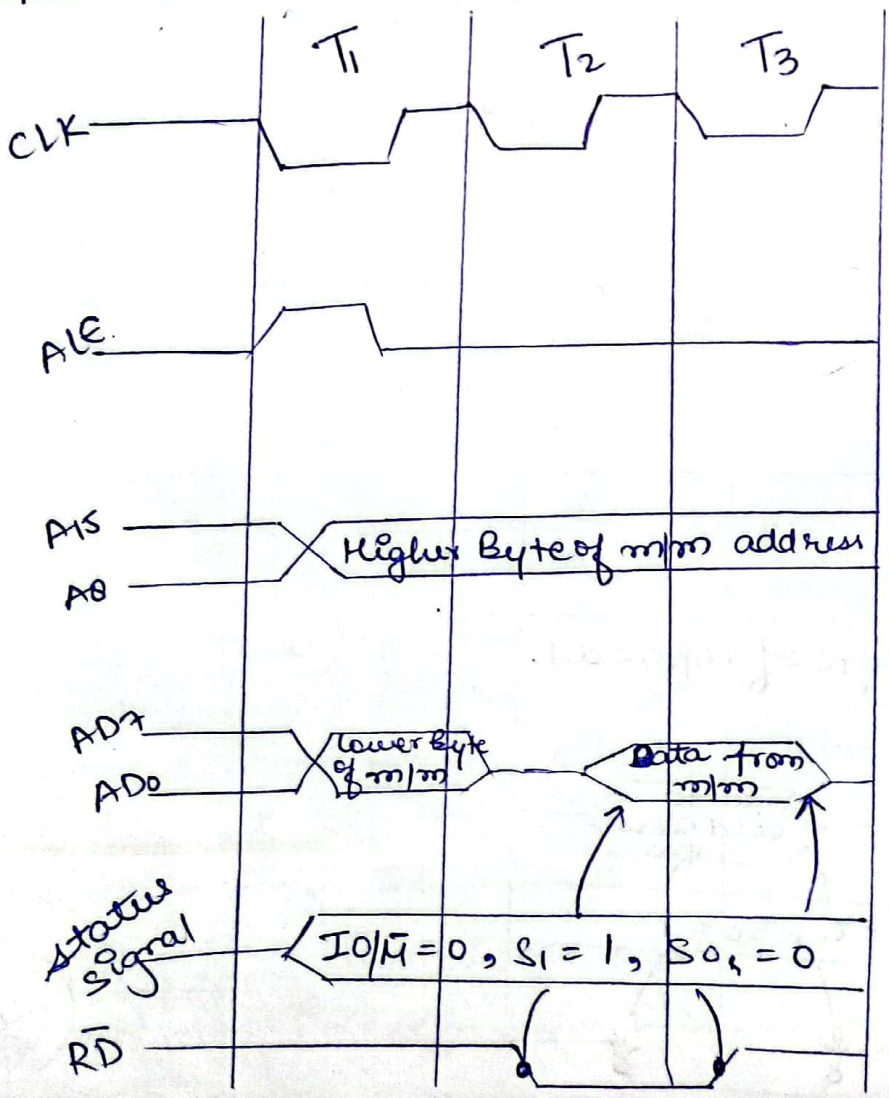
ALE enable the address latch and address latch load 16 bit m/m address on higher order Bus multiplexed with Data Bus. Up also set status signal $IO/\overline{M}=0$ $S_1=1, S_0=1$.

During T_2 → The higher Byte of m/m address retain AD_8-AD_{15} and lower Byte of m/m address AD_0-AD_7 goes in Tri-state logic and up enable control signal $\overline{RD}$. The opcode from m/m start to load on add-data Bus

During T_3 → When complete opcode loaded on data Bus up disable $\overline{RD}$ signal and data Bus goes in Tri-state logic

During T_4 → The opcode of inst is stored in inst register which is transfer to inst. decoder and m/c cycle encoder. The decoded opcode transfer to timing and control unit for op. or next m/c cycle generation.

M/M Read Machine cycle:



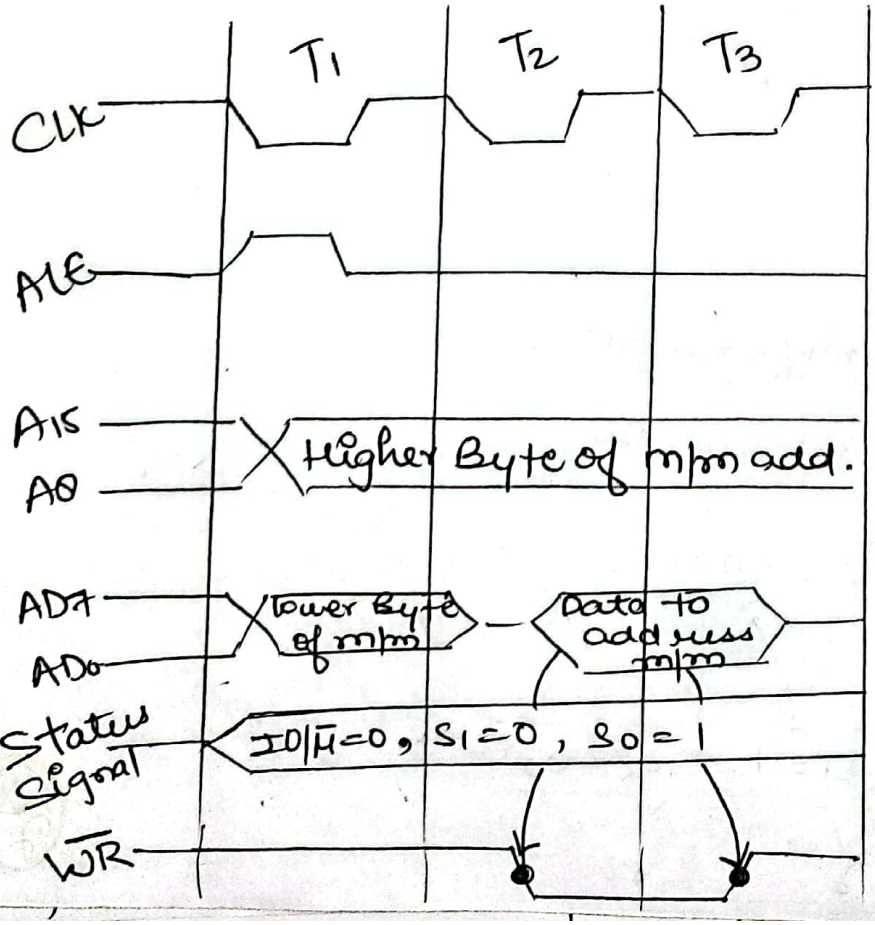
Up ~~read~~ perform read m/c cycle to read the content of add. m/m location. It consume three T-state In this Up place the content of SP, register pair or PC on add. Bus. The timing diagram shown in fig.

During T_1 → Up enable a ALE signal for instant of time. which enable address latch distribute 16 bit m/m add in two parts and load higher order add. Bus and multiplexed data Bus and Up also set Status signal $IO/\overline{M} = 0$, $S_1 = 1$, $S_0 = 0$. By this it ~~indicate~~ indicate m/m m/c cycle.

During T_2 → Higher Byte of m/m add retain on A8 - A15 and lower Byte m/m address disappear.
Up enable control signal $\overline{RD}$ and data from add. m/m begins to load on Data Bus.

During T_3 → When complete data loaded on Data Bus. Up disable control signal $\overline{RD}$.

• M/m Write Machine cycle:



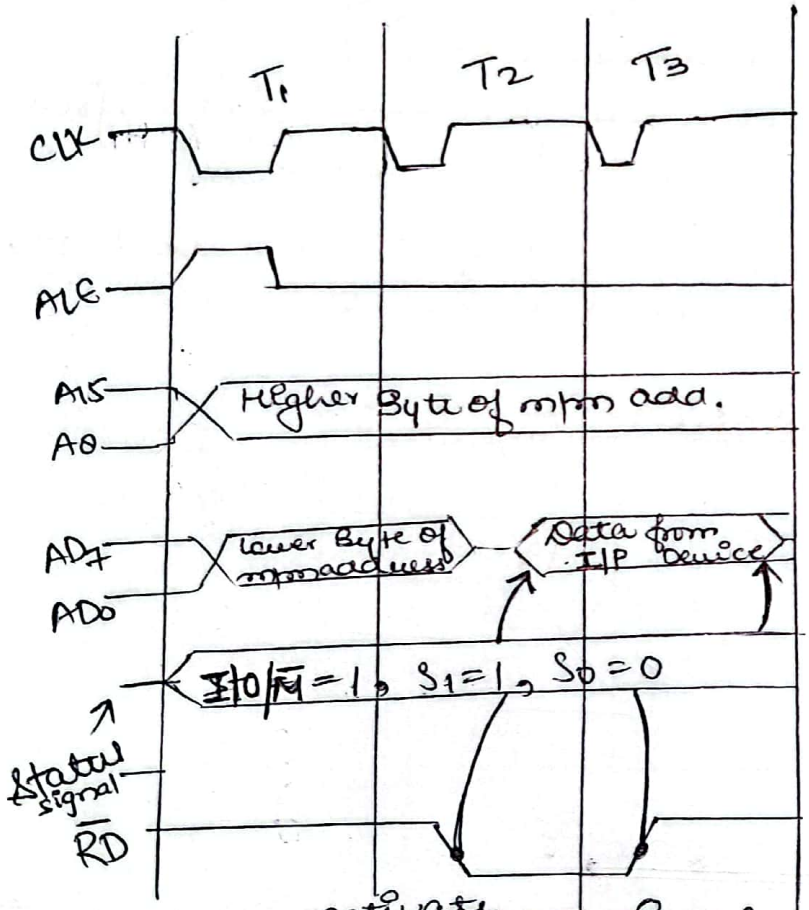
The timing diagram of m/m write is similar to m/m read m/m cycle. It also consume 3 Time State as shown in figure. The changes from difference m/m ~~read~~ write m/m cycle is as follows—

During T_1 → Mp sets $IO/\overline{M}=0$, $S_1=0$, $S_0=1$ for m/m write

During T_2 → Mp enable $\overline{WR}$ in place of $\overline{RD}$ and data start to store at addressed m/m location.

During T_3 → When comple data store in m/m Mp disabled the $\overline{WR}$ signal.

I/O Read machine cycle :



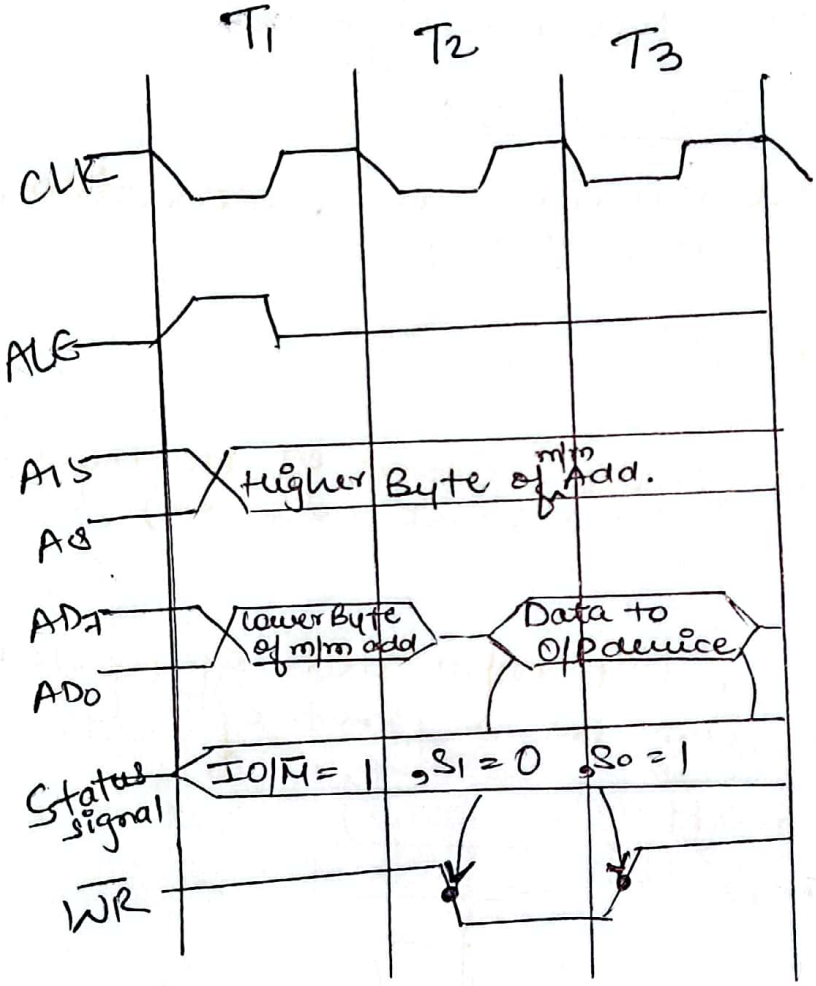
During T_1 → Mp ~~enable~~ activate ALE signal which enable address latch. Add. latch load higher Byte of m/m add on A0–A15 pin and lower Byte on AD0–AD7 Mp also set status signal $IO/\overline{M}=1$, $S_1=1$, $S_0=0$ To identify Io read op.

During T_2 → The lower Byte of m/m add. disappears from multiplexed data Bus and it goes in

Tristate logic for restart of time. µp activate RD control signal and data from address I/P port to start to load on data Bus.

During T_3 → µp disable RD signal when complete data loaded on data Bus and IO Read m/c cycle terminated.

I/O Write Machine Cycle:



#Addressing Modes:

Every inst of a program operate on data it is c/d operand so the method of specifying in an inst is c/d addressing & different techniques of providing operand is termed as mode. Operand may a direct data, data stored in register, data stored in m/m or data input from Input device.

8085 µp has five addressing Modes —

- **Immediate AM:**

The 8 bit or 16 bit data is specified in the inst. as a part of inst. and inst. having letter 'I' is opcode.

```
MVI B, 20H
MVI M, 30H
LXI D, 20FFH
```

- **Register AM:**

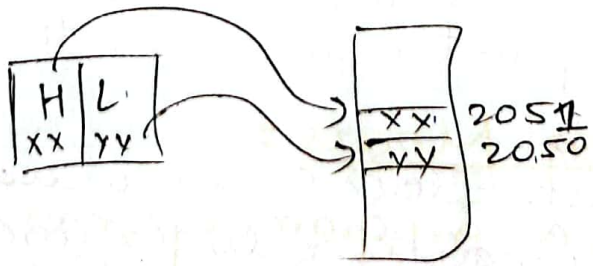
In this mode the source and destination operand is register as a part of inst.

```
MOV B, A
ADD B
SP HL (Moves content of HL register pair
       into stack pointer).
```

- **Direct AM:**

In this mode the 16 bit mem add. of operand is specify in the inst as a part of inst.

```
LDA 2500H
SHLD 2050H
```



- **INDirect AM:**

In this AM the add of mem stored in register & register is specified in inst.

```
LDAX B
MOV M, A
```

- **Implied AM:** The opcode specify the add. of operand.

*Instruction set of 8085 Up:

Up performs its op. acc to the codes written in its m/m i.e, called Inst. A group of Inst. is known as a program i.e, written in assembly lang. Up approx. 4@50 types of Inst. each all Inst classified in 5 different groups based on the nature of func. formed by them. These 5 groups are c/d Inst set of Up which are :-

(1) Data Transfer Group
(2) Arithmatic Group
(3) Logical Group
(4) Branch Group
(5) Input | output, stack and machine control group.

- **Data Transfer Group:**
Data transfer group Inst. are used to store data into registers, copy data from register to m/m & vice-versa.

- **Arithmatic Group:**
This group Inst. performs arithmatic op. like addition, subtraction, Increment & decrement of data. This group Inst. affect all the flags of flag registers.

- **Logical Group:**
This group Inst. performs logical op. like rotate, compare, compliment, AND, OR, NOT and Ex-OR op. This group Inst. also affects the flags.

- **Branch Group:**
This group Inst. allows a Up to change a sequence of program conditionally or unconditionally. The main Inst. of this group are jump & call & return Inst.

- **Input/output, stack & m/c control Group:**
This group Inst. controls periferal devices, Up op. like Interrupt, Halt or no op. and direct use of large no. of data stored in a portion of m/m.

#Instruction format:

Each Inst of 8085 Up Microprocessor have specific info, the operand on which the operation to be performed acc to the info the inst are classified are in three categories —

• One Byte Instruction:

Such Insts are consist only opcode and the source and destination as a part of opcode & such Inst are stored on a ~~pa~~ single m/m add. (location) Ex: MOV A, B

• Two Byte Instruction:

In such Inst. the 8 bit data ~~the~~ specified in Inst after the opcode the 8 bit data of may be direct data or I/O port address Ex: MVI B, 25H

• Three Byte Instruction:

A 16 bit data of m/m add are specified in the Inst. along with the opcode such Inst are 3 byte Inst. Ex: JMP 6200H

#Opcode format:

Each Inst. of 8085 Up has a 8 bit opcode which contain info. about the operation and each opcode is unique for each Inst. The format of opcode is as follows:

Function	Opcode		
	Operation Info.	Destination Register code	Source Register code.
MOV r_d, r_s A, B	B_7 B_6 0 1	B_5 B_4 B_3 1 1 1	B_2 B_1 B_0 0 0 0
MVI r, data(8)	0 0	0 0 0	1 1 0

Table for Register Code:

Register	Code	Register Pair	
B	000	BC	00
C	001		
D	010	DE	01
E	011		
H	100	HL	10
L	101		
Memory (M)	110	AF & SP	11
A	111		

#Interrupts:

The 8085 interrupt process control by interrupt enable flip flop. It is internal process in the processor and it can be set or reset by using software inst. if this flip flop is enable and interrupt signal INTR receives logic 1 then the processor is interrupted.

Types of Interrupt:

Interrupts are basical two types:

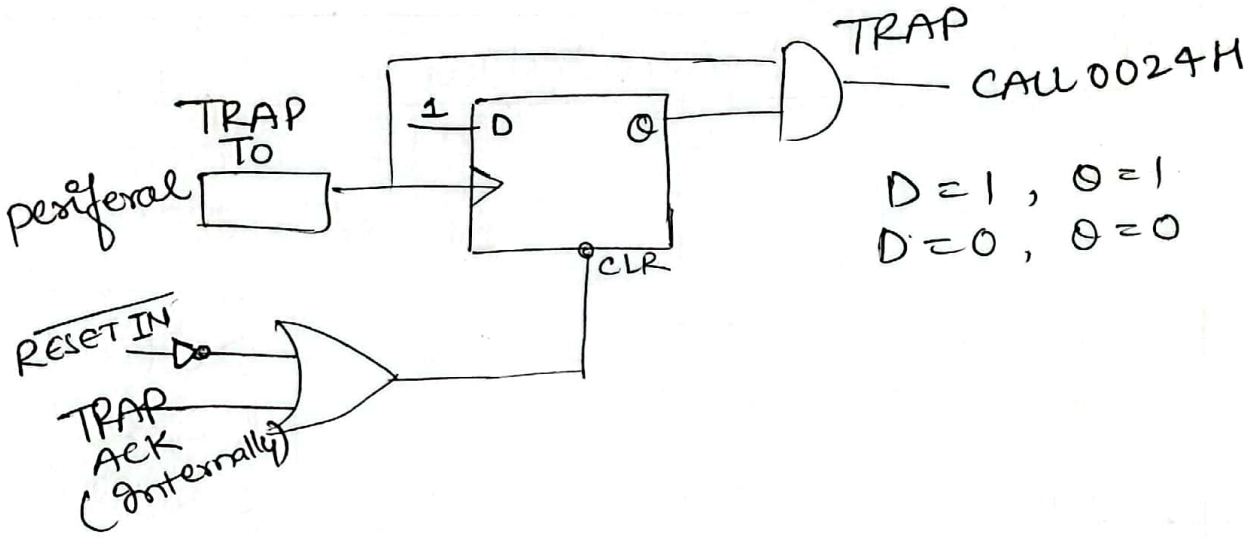
Hardware Interrupt:

8085 have 5 interrupt pin allow the perferal devices to interrupt main program for I/O related op. When interrupt request occur it complete the current inst & transfer the program control to a service subroutine of periferal device. 8085 has 5 pins TRAP, RST7.5, RST6.5, RST5.5, INTR, according to the priority. TRAP is highest priority it is non-maskable interrupt (It cannot enable or disable by programmer)

(82)

TRAP:

This interrupt enabled by edge triggering or level triggering and it maintain until it is acknowledge.



The fig shows TRAP interrupt ckt. A positive edge signal D flip flop and due to AND Gate it sustain high level on its output. There are two ways to clear TRAP interrupt by reseting the up (to give RESET IN signal) and by generating TRAP acknowledge signal high (Internally).

RST 7.5:

It is second highest priority interrupt. It can be clear by inst. SIM of by Internally generated acknowledgement signal.

RST 6.5 and RST 5.5:

These are third and fourth highest priority Interrupt These are also vectored interrupt bcz when these interrupts are enabled the program control shift to a fix m/m add. for RST 6.5, the vectored add. is 0034 H and for RST 5.5, the Vectored add. is 0026 H and these interrupt mask by SIM inst.

INTR (Interrupt request signal):

INTR is a maskable interrupt & non-vectored Interrupt It has least priority. up continue check status of INTR signal. when this signal goes high up complete current inst and activate $\overline{INTA}$ signal.

Software Interrupt:

8085 µp has 8 s/w Interrupt from RST 0 TO RST 7.
The vectored add. from these Interrupt can be calculated as
Interrupt No × 8 = Vector Address.

Interrupt	Machine Code/Hexa Code	Vector Address
RST 0	C7	0000H
RST 1	CF	0008H
RST 2	D7	0010H
RST 3	DF	0018H
RST 4	E7	0020H
RST 5	EF	0028H
RST 6	F7	0030H
RST 7	FF	0038H

~~RST 0~~

The s/w Interrupts are program Inst which inserted at desired location in a program when Interrupt Inst execute the µp transfer the program Control/program execution to Vectored add. of the Inst..

Vectored Interrupt:

When the Interrupt signal activate or Interrupt Inst. execute µp Internal ckt produces the Call Inst ~~the~~ for predetermine m/m add is c/d Vector Interrupt. (predetermine m/m location is c/d Vectored add).

Instruction Set:

S.No	Instruction	operation	flag	No. of Byte	M/cycle	No. of T-state	Addressing Modes
1.	MVI r, data(8)	data(8) → r	No	2	OF+MR	4+3=7	Immediate
2.	MVI m, data(8)	data(8) → $(M)_{HL}$	No	2	OF+MR+MW	4+3+3=10	Immediate Indirect
3.	MOV rd, rs	rs → rd	No	1	OF	4	Register
4.	LXI rp, (16)data	16 bit data → rp		3	OF+MR+MR	4+3+3=10	Immediate
5.	STA addr	A → (addr)		3	OF+MR+MR+MW	4+3+3+3=13	Direct
6.	LDA addr	(addr) → A		3	OF+MR+MR+MR	4+3+3+3=13	Direct
7.	SHLD addr	L → (addr) H → (addr+1)		3	OF+MR+MR+MW+MW	4+3+3+3+3=16	Direct
8.	LHLD addr	L ← (addr) H ← (addr)		3	OF+MR+MR+MR+MR	16	Direct.
9.	STA X rp	A → (rp) addr		1	OF+MW	7	Indirect
10.	LDA X rp	(rp) → A		1	OF+MR	7	Indirect
11.	XCHG	L ⇌ E H ⇌ D		1	OF	4	Register