Unit - 2

TRANSISTORS ...

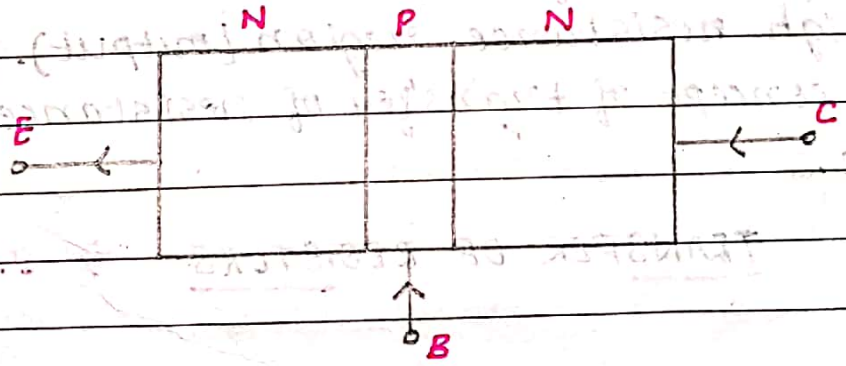
* Bi-Polar Junction Transistor (BJT) :-

- It is a three terminal device named as emitter, base, collector.
- The conduction of current takes place due to majority as well as minority charge carriers, that's why it is called Bi-Polar Junction Transistor.

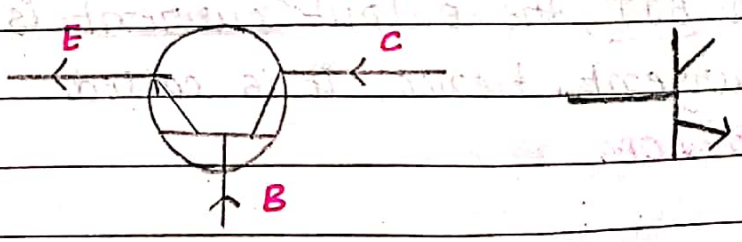
*⇒ Types of BJT :-

(a) NPN
(b) PNP

*⇒ Construction of NPN :



Symbol ⇒



- It is formed by sandwiching ~~between~~ a thin p-type semi-conductor between two thick n-type semi-conductor.

- It has three terminals, i.e. Emitter, Base and Collector, where Base terminal comes between emitter and collector, and also Base is thin and lightly doped.

- Emitter and collector are much wider than base and they are heavily doped, emitter is heavily doped than collector.

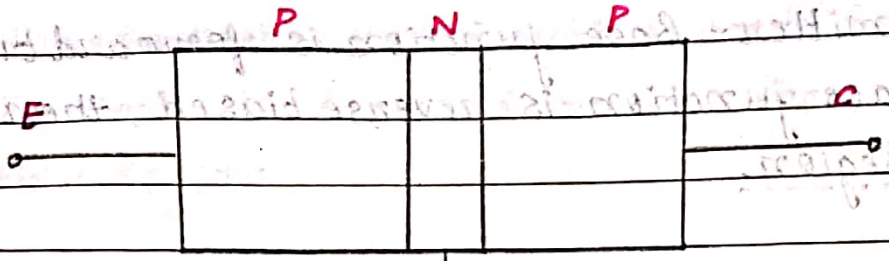
Ques Define Transistor.

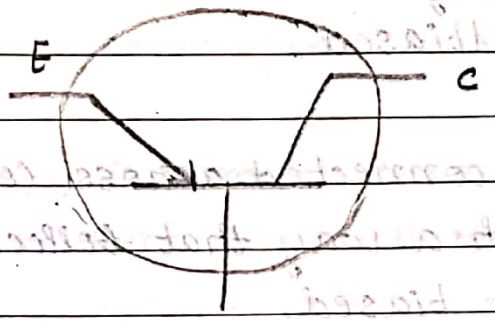
Ans ⇒ It is a three terminal device (Emitter, base, collector)
⇒ Depending upon the configuration it can be used as voltage as well as current amplification.
⇒ It can be used as voltage as well as current amplification.
⇒ The ampiification in the transistor is achieved by passing input signal from low resistance region to high resistance region (output).
⇒ The concept of transfer of resistance is known by the name.

TRANSFER OF RESISTORS ⇒ TRANSISTORS

In BJT, the output current is controlled by the input current. Hence, it is called CURRENT CONTROLLING DEVICE.

* Construction of PNP :-





⇐ Symbol

* Biasing of Transistors : (BJT)

⇒ When an external DC voltage is applied across the different terminals of the transistors is called Biasing.

⇒ Depending upon the DC applied voltage polarities, across the junction, the transistor work in three modes of operation.

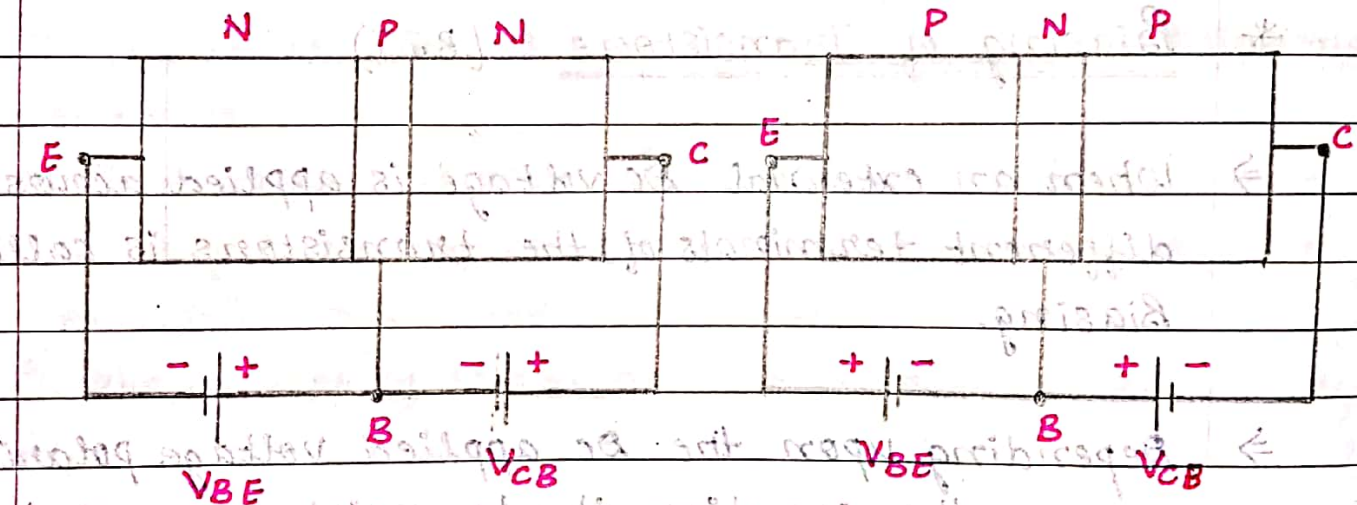
MODE	Emitter-Base Junction	Collector-Base Junction
Active	Forward Bias	Reverse Bias
Saturation	Forward Bias	Forward Bias
Cut-Off	Reverse Bias	Reverse Bias

Active Region :-

⇒ Emitter - Base junction is forward biased and collector base junction is reverse biased, then it is Active Region.

⇒ Battery V_{BE} is connected across Emitter - Base Junction in such a way that Emitter - base junction becomes forwardbiased.

⇒ Battery V_{CB} is connected across Collector - Base Junction in such a way that Collector - base junction becomes reverse biased.



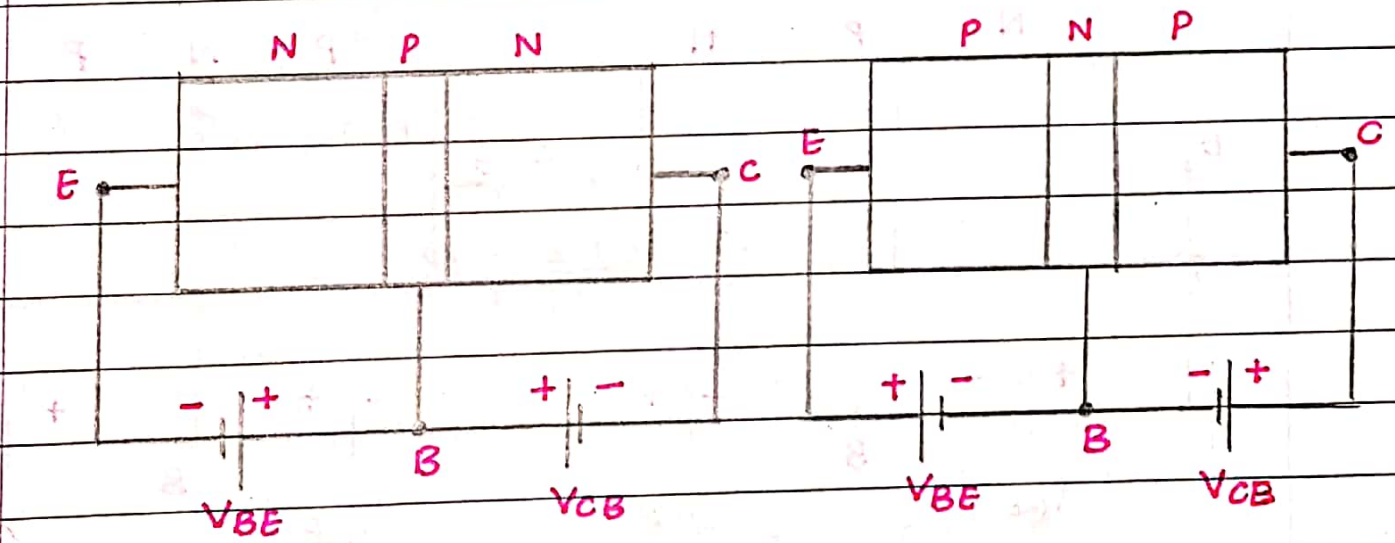
⇒ In this region, the collector current 'I_C' depends upon the emitter current 'I_E' and transistor work as an Amplifier.

• SATURATION REGION :-

⇒ Both the Emitter - Base Junction and Collector - Base Junction is forward biased, then it is Saturation Region.

⇒ Battery V_{BE} is connected across Emitter - Base Junction in such a way that Emitter - base junction becomes forward bias.

⇒ Battery V_{CB} is connected across collector - base junction in such a way that collector - base junction becomes forward bias.



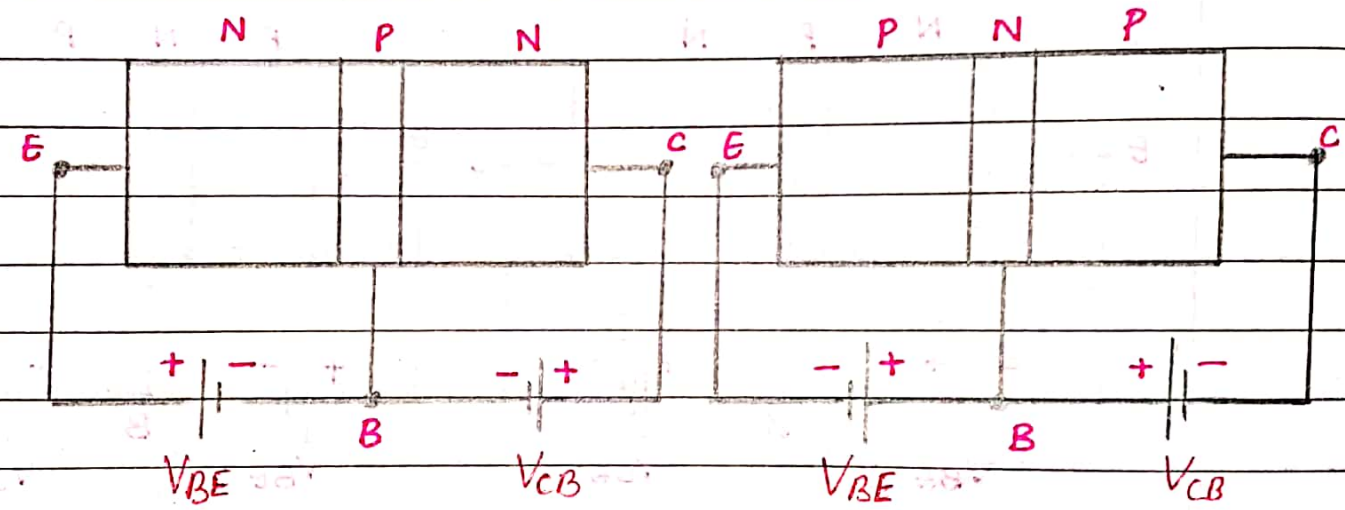
⇒ The collector current 'I_c' becomes independent of the base current 'I_B' and transistor acts as a closed switch (i.e. short circuit).

CUT-OFF REGION :-

⇒ Both the Emitter-Base Junction and Collector-base Junction is reverse biased, then it is cut-Off Region.

⇒ Battery V_{BE} is connected across Emitter-Base Junction in such a way that Emitter-base junction becomes reverse biased.

⇒ Battery V_{CC} is connected across Collector-Base Junction in such a way that Collector-base junction becomes reverse biased.



⇒ In this region, transistor is used as an open switch.

Ques For a N-P-N transistor $I_E = 12\,mA$ and $\beta = 140$. Determine the value of I_B and I_C.

Ans $\beta = \frac{I_C}{I_B}$ $\qquad I_E = I_B + I_C$

$I_C = 12 - I_B$

$140 = \frac{I_C}{I_B}$

$140 I_B = 12 - I_B$

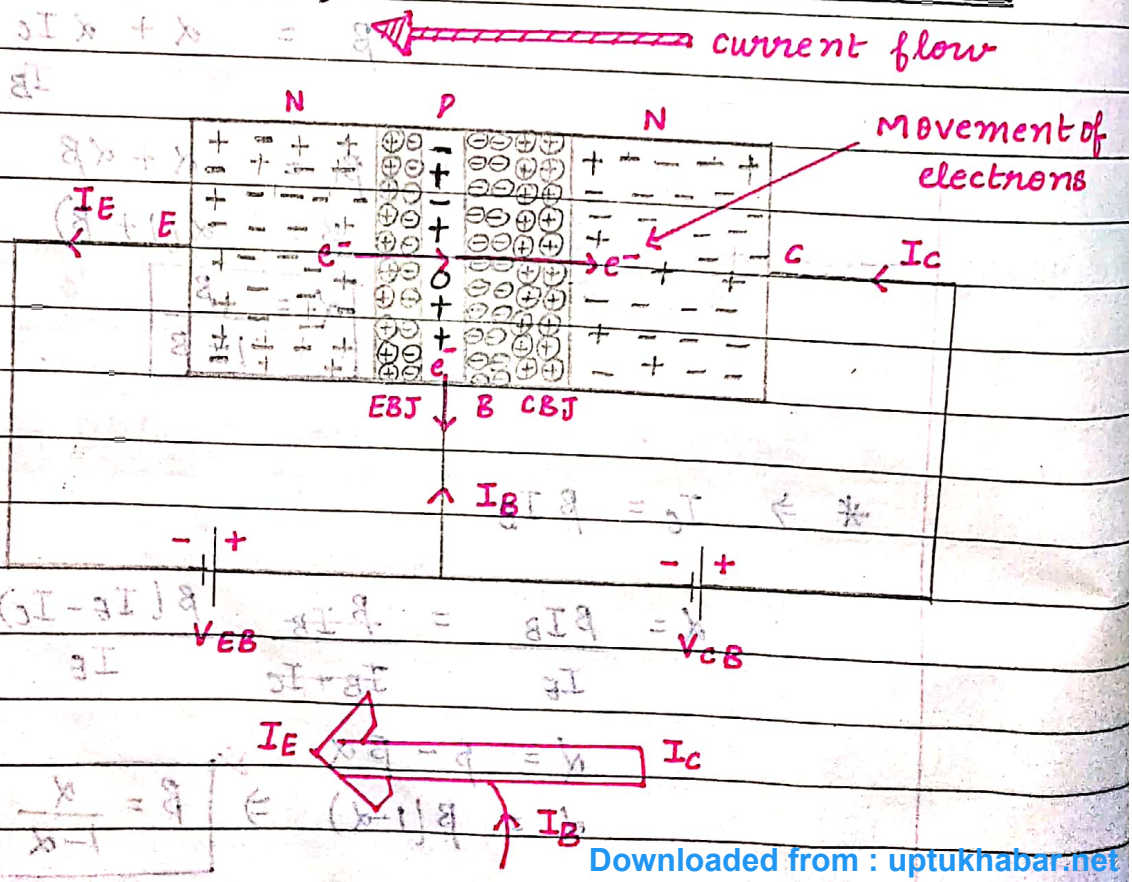
$141 I_B = 12$

$I_B = 0.085\,mA$

$I_C = 12 - 0.085 = 11.914\,mA$

$\alpha = \frac{I_C}{I_E} = \frac{11.914}{12} = 0.992$

* Operation of N-P-N Transistor :



$$I_E = I_C + I_B$$

⇒ The Emitter - Base Junction is forward biased by the DC source V_{EB}, thus, the depletion region across it is reduced. The collector - Base Junction is reverse biased and due to this the depletion region will be increased across it as shown in the figure.

⇒ The forward biased Emitter - Base Junction causes the electron in the N-type emitter to flow towards the base. And this generates the emitter current I_E.

⇒ Due to light doping, very few no. of electrons injected into the base from the emitter recombine with holes to produce base current I_B. And remaining large no. of electrons crosses the Collector - Base Junction.

⇒ This produces collector current I_C, thus, the e⁻ flow produces the dominant current in a N-P-N transistor.

⇒ Since, most of the electrons from emitter flow in the collector circuit and very few combine with the holes in the base. Thus, the collector current is larger than the base current and the relation between these currents is given by -

$$I_E = I_C + I_B$$

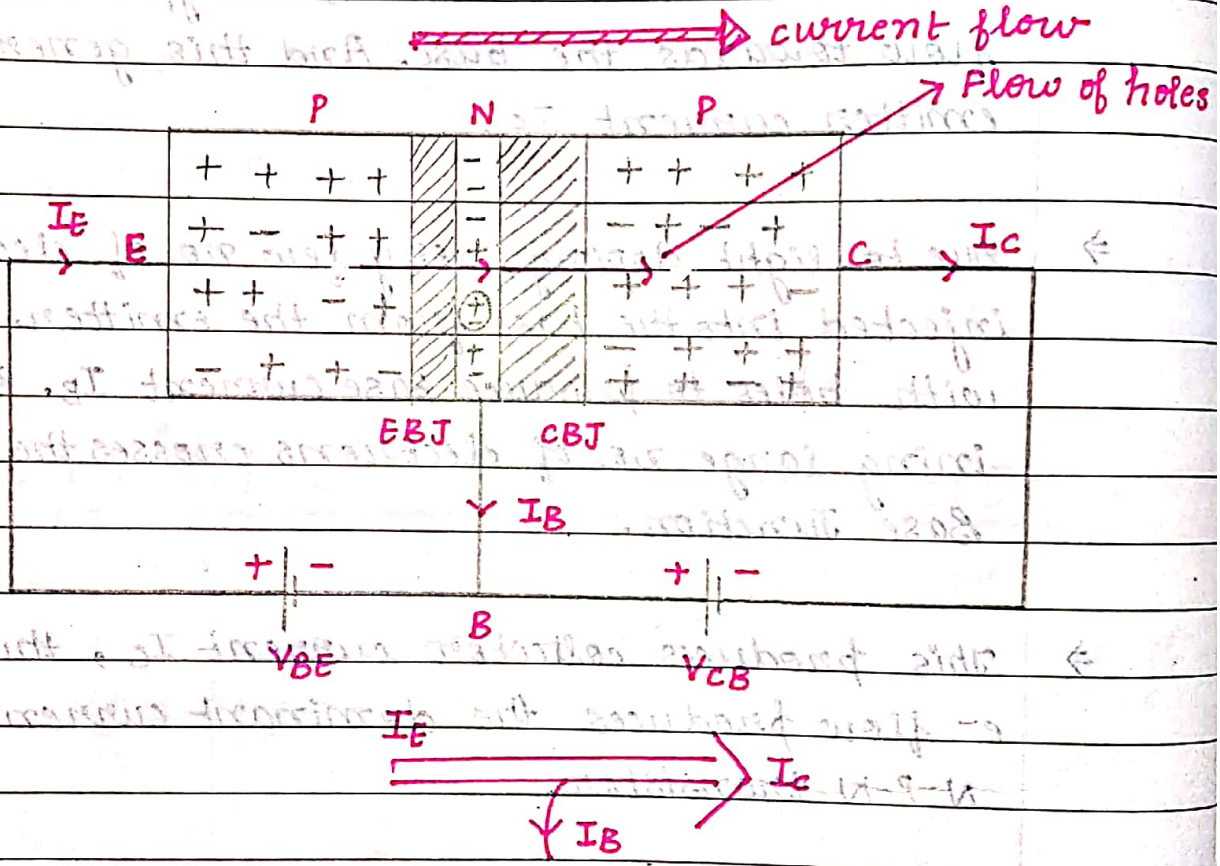
⇒ Since, it is a bipolar device, the collector current

includes two components - majority and minority, where minority current component is called Leakage current and is given by - I_{CO} or I_{CBO} (I_C current with emitter terminal open)

$$I_C = I_{C(majority)} + I_{C(minority)}$$

$$\Rightarrow \boxed{I_C = I_{C(maj)} + I_{CO}}$$

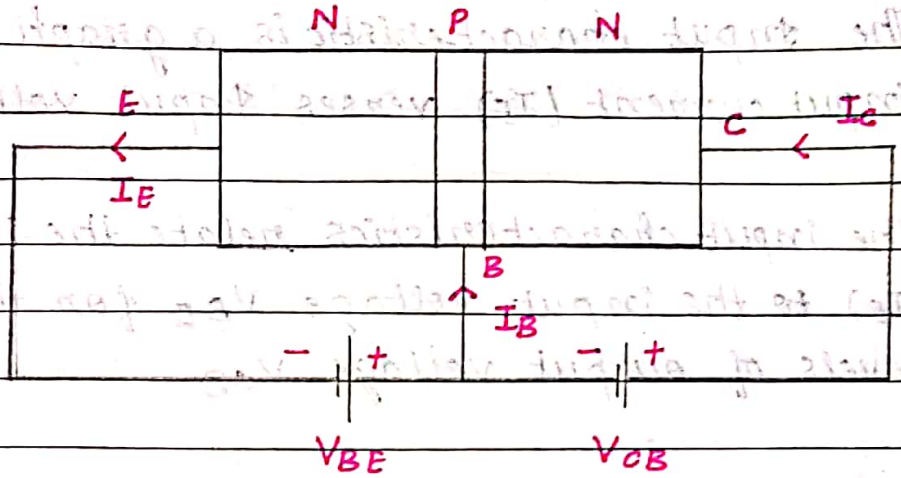
* Operation of P-N-P Transistor :-

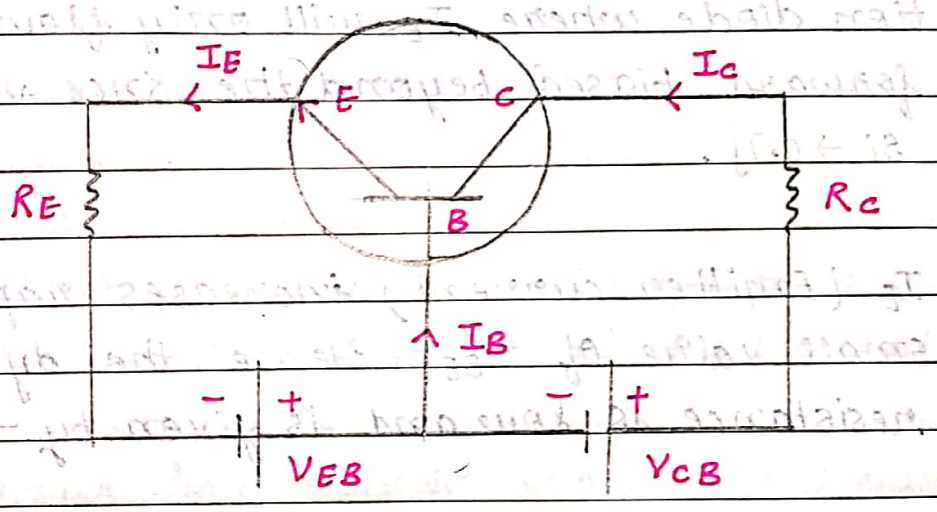


$$\boxed{I_E = I_C + I_B}$$

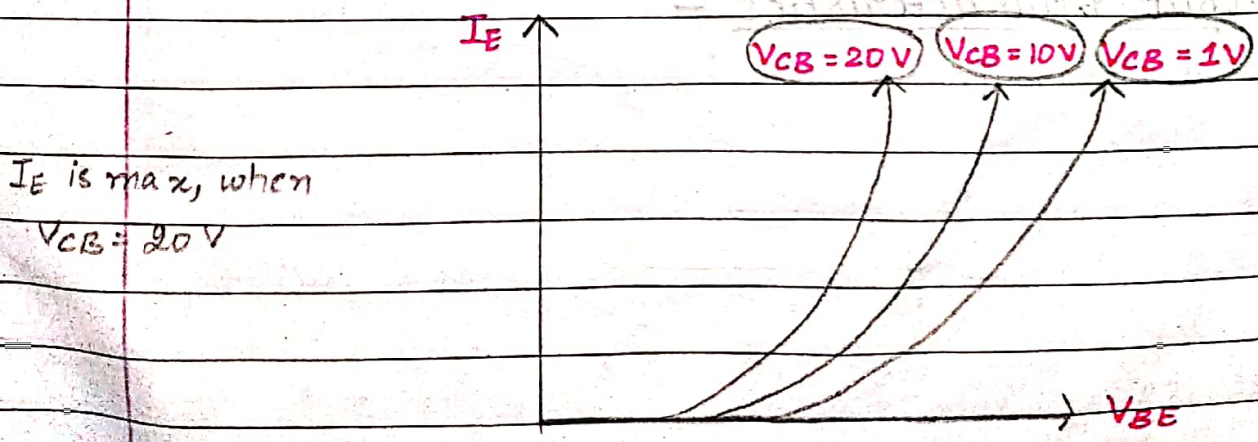
The Emitter - Base Junction

* Common Base Configurations





In common-Base configuration, the base is common between both the input as well as output side as shown in the figure.



I_E is max, when $V_{CB} = 20V$

- **Input Characteristics –**

→ The input characteristic is a graph between input current (I_E) verses input voltage (V_{BE}).

→ The input characteristics relate the input current I_E to the input voltage V_{BE} for the various levels of output voltage V_{CB}

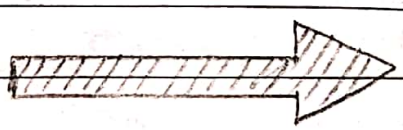
→ It is similar to the VI-characteristics of pn-junction diode where I_E will only flow when V_{BE} is forward biased beyond the Knee voltage [Ge → 0.3 Si → 0.7].

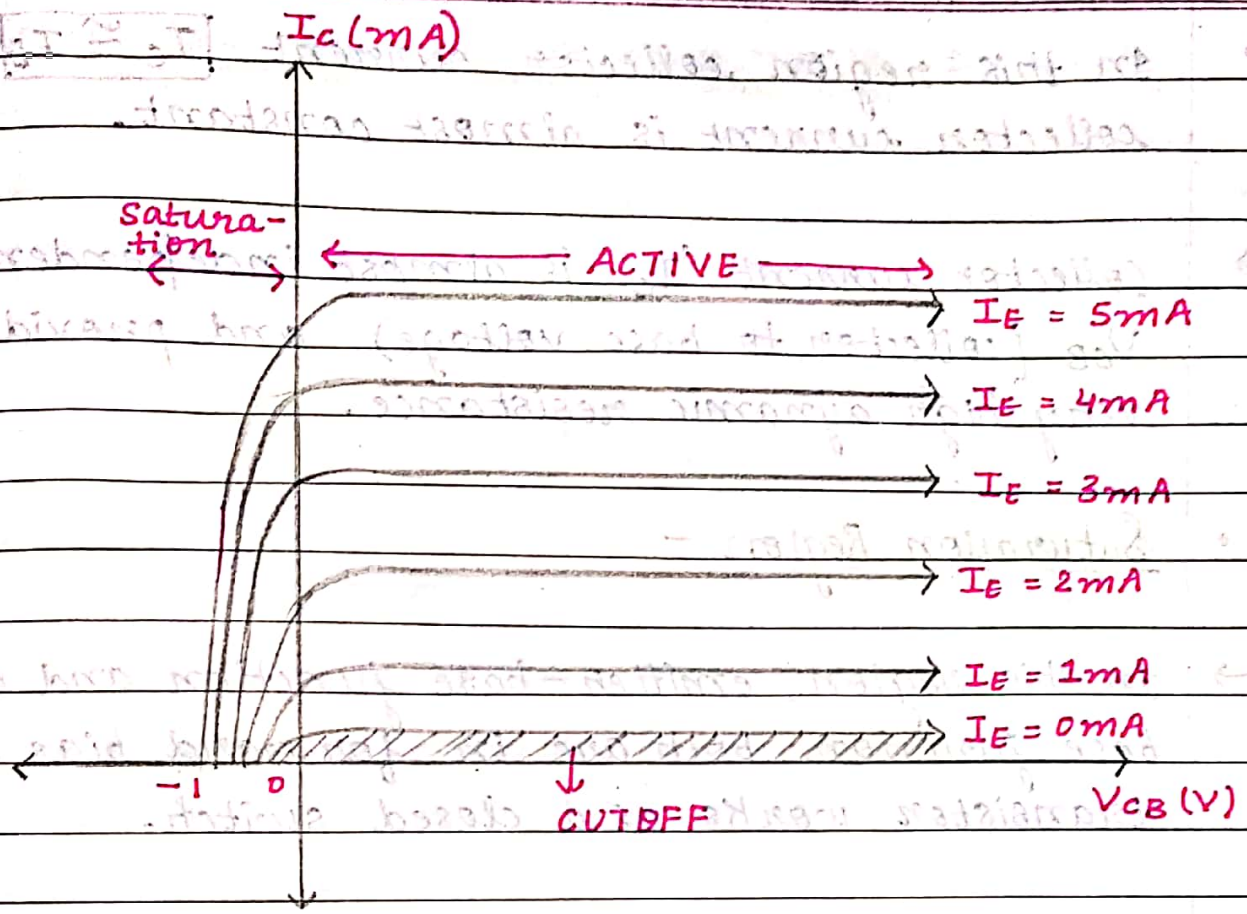
→ I_E (Emitter current) increases rapidly with a small value of V_{BE}. Hence, the dynamic input resistance is low and is given by –

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_E}\right|_{V_{CB} = \text{constant}}$$

r_i → dynamic resistance

- **Output Characteristics –**





→ The output characteristics is a graph between the output current (I_C) verses output voltage (V_{CB}).

→ The output characteristics shows the relation between output current I_C verises the output voltage V_{CB} for the various levels of input current, I_E.

→ The dynamic output resistance 'r_o' is given by —

$$r_o = \left.\frac{\Delta V_{CB}}{\Delta I_C}\right|_{I_E = \text{constant}}$$

• Active Region —

→ In this region, Emitter-base junction is forward biased and collector-base junction is reversed bias and transistor acts are amplifier.

→ In this region collector current $I_C \cong I_E$ and collector current is almost constant.

→ Collector current 'I_C' is almost independent of V_{CB} (collector to base voltage) and provides very high dynamic resistance.

- **Saturation Region –**

→ In this region, emitter-base junction and collector base junction both are in forward bias and transistor works as a closed switch.

→ In this region, collector current I_C is independent of emitter current I_E.

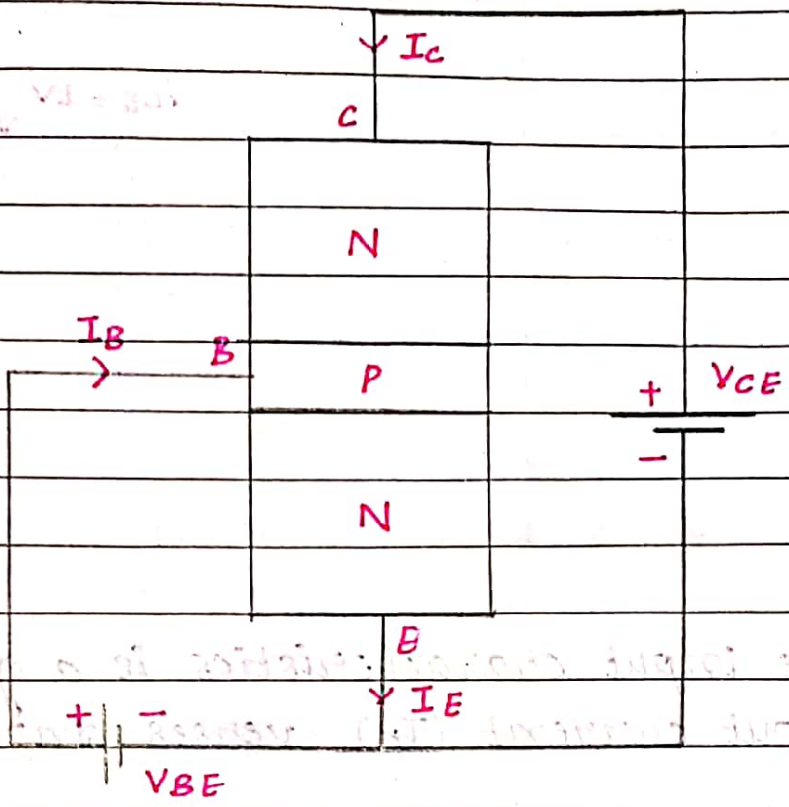
→ In this region V_{CB} is negative (–ve) and I_C decreases rapidly when V_{CB} becomes more negative (–ve).

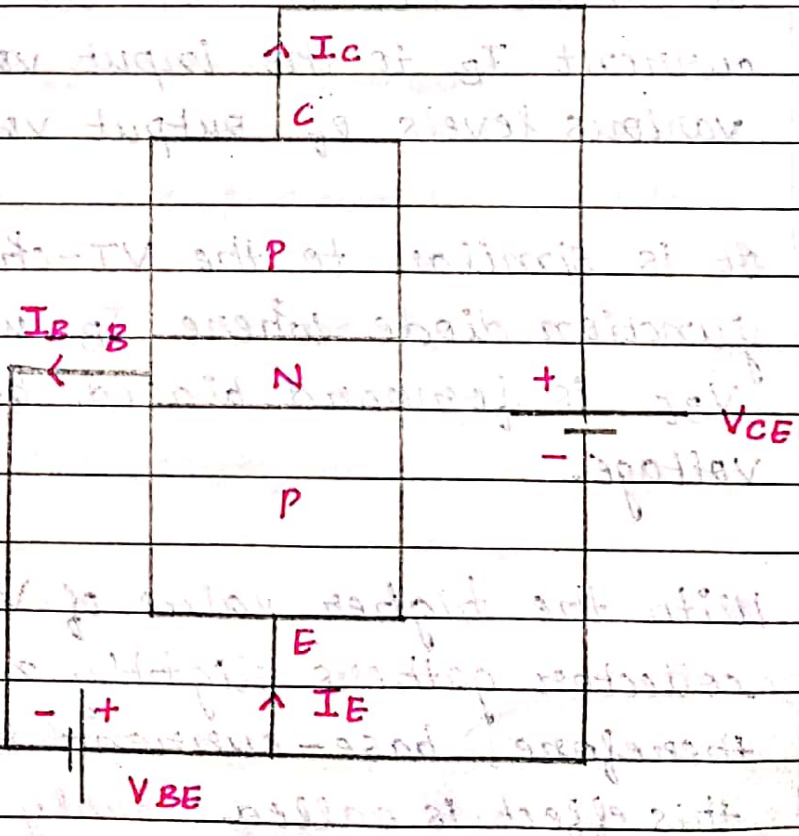
- **Cut-off Region –**

→ Collector-base junction and emitter-base junction both are in reverse bias and transistor works as a open switch.

→ The region below $I_E = 0\,mA$, is known as cutoff region where collector current is approximately 0.

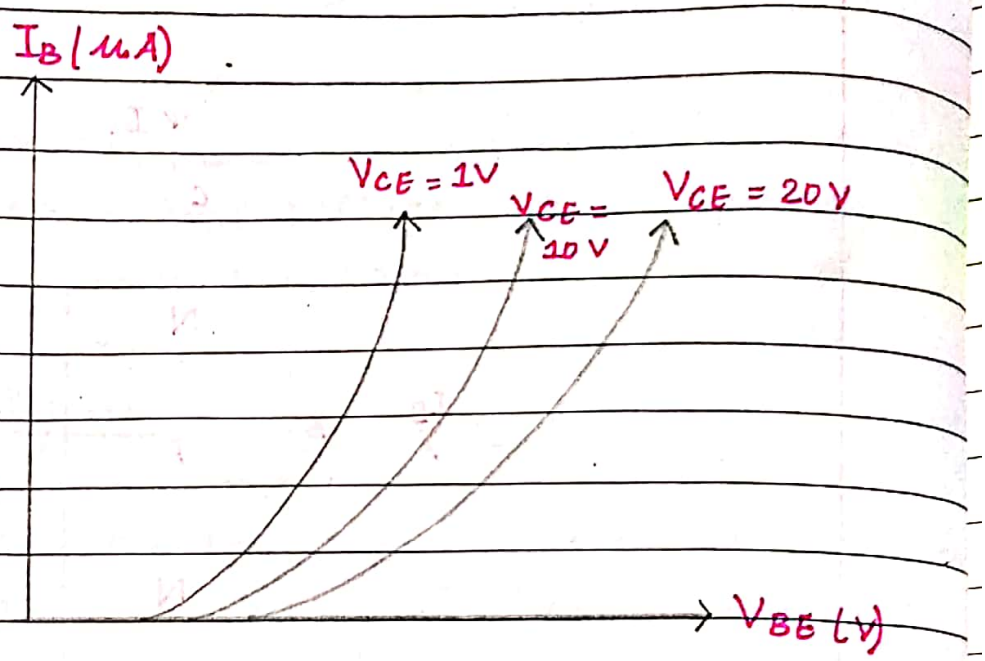
* COMMON EMITTER CONFIGURATIONS :-





In common-emitter configuration, the emitter is common between both input as well as output side as shown in the figure.

- **Input characteristics of**



→ The input characteristics is a graph between input current (I_B) verses input voltage (V_{BE}).

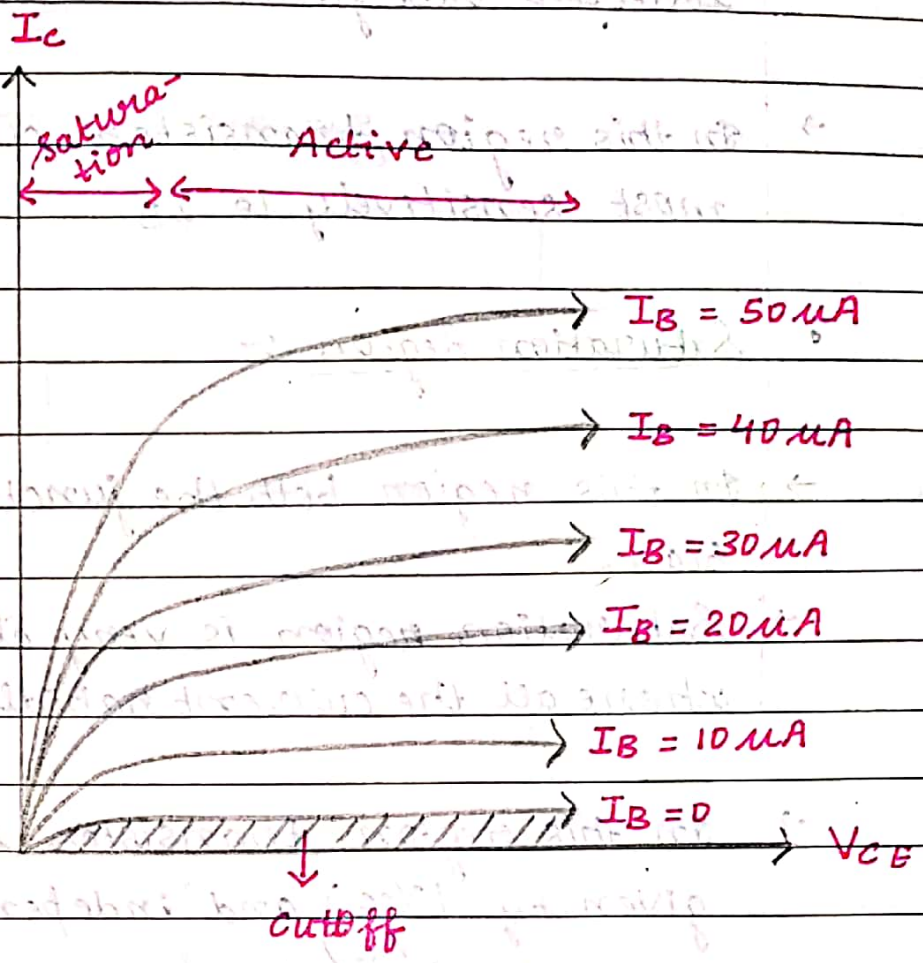
→ It shows the relation between the input current I_B to the input voltage V_{BE} for the various levels of output voltage V_{CE}.

→ It is similar to the VI-characteristics of pn-junction diode where I_B will only flow when V_{BE} is forward biased beyond the Knee voltage.

→ With the higher value of V_{CE} (output voltage), collector gathers slightly more electrons and therefore, base-current reduces. Normally, this effect is called Early effect which is generally neglected.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \Big| \quad V_{CE} = \text{constant}$$

• Output Characteristics :-



$$I_{CEO} = (1+\beta) I_{CBO}$$

→ It is the graph between output current I_C v/s output voltage V_{CE}.

→ It shows the relation between I_C v/s V_{CE} for the various levels of I_B.

→ Dynamic output resistance,

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B = \text{constant}}$$

• Active Region :-

→ In this region emitter base junction is forward bias and collector base junction is reversed biased.

→ For the fixed value of I_B, as we increase V_{CC} the collector base junction current increases rapidly.

→ In this region, transistor current i.e. I_C responds most sensitively to I_B.

- **Saturation Region :-**

→ In this region both the junction are in forward bias.

→ Saturation region is very close to zero access where all the current rapidly reduces to zero.

→ In this region, transistor collector current is given by $\left(\frac{V_{CC}}{R_C}\right)$ and independent of base current.

- **Cut Off Region :-**

→ In this region, both the junctions are reverse bias.

→ The region below, $I_B = 0$, is know as cut off region.

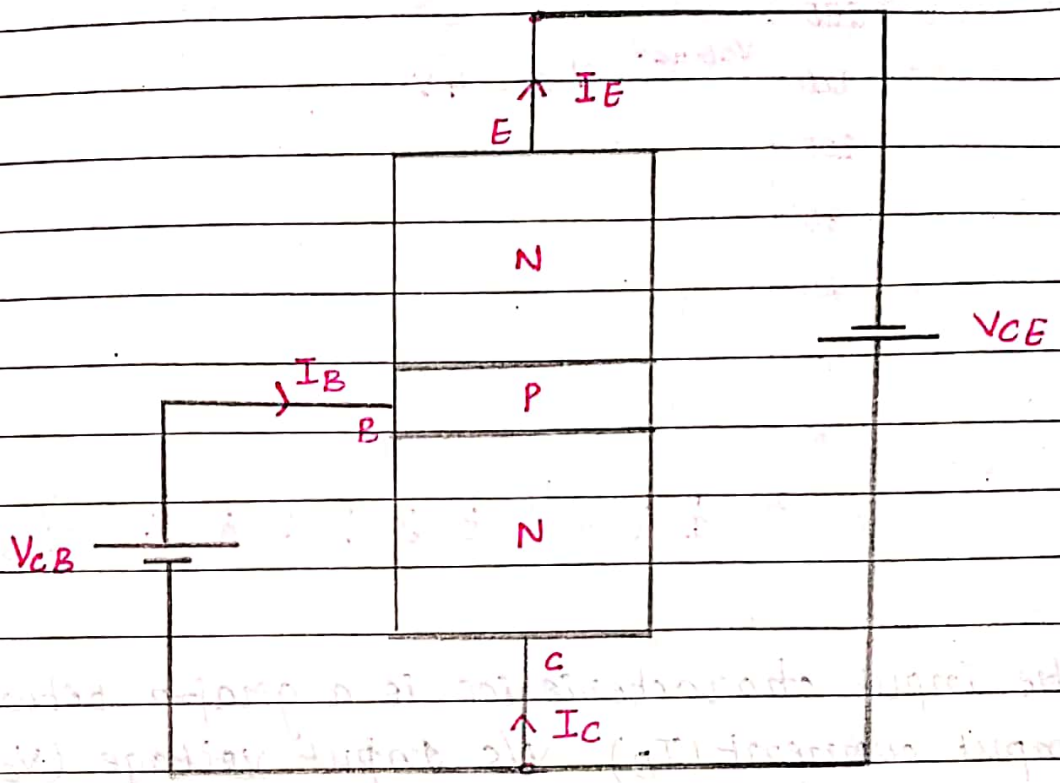
→ When I_B becomes zero then I_C is approximately equal to I_{CEO} and is given by -

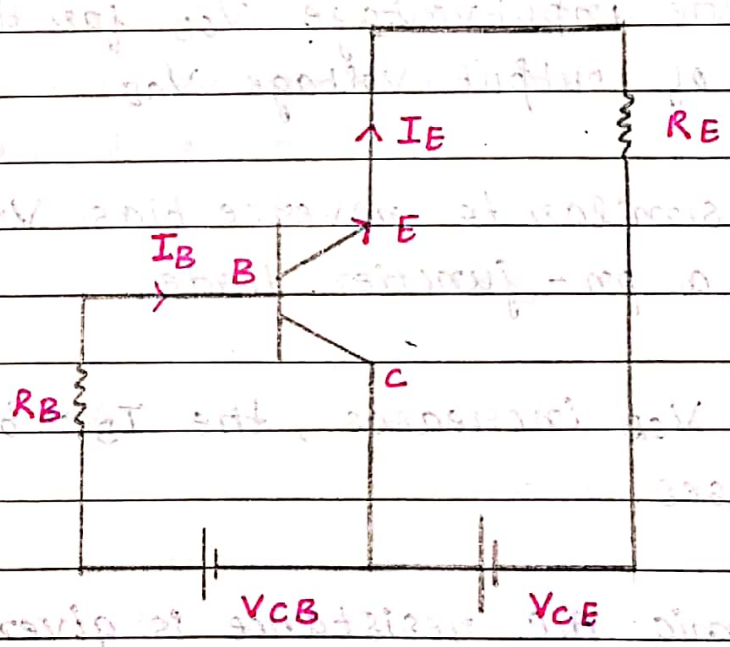
$$I_{CEO} = (1 + \beta) I_{CBO}$$

* COMMON COLLECTOR CONFIGURATIONS

OR

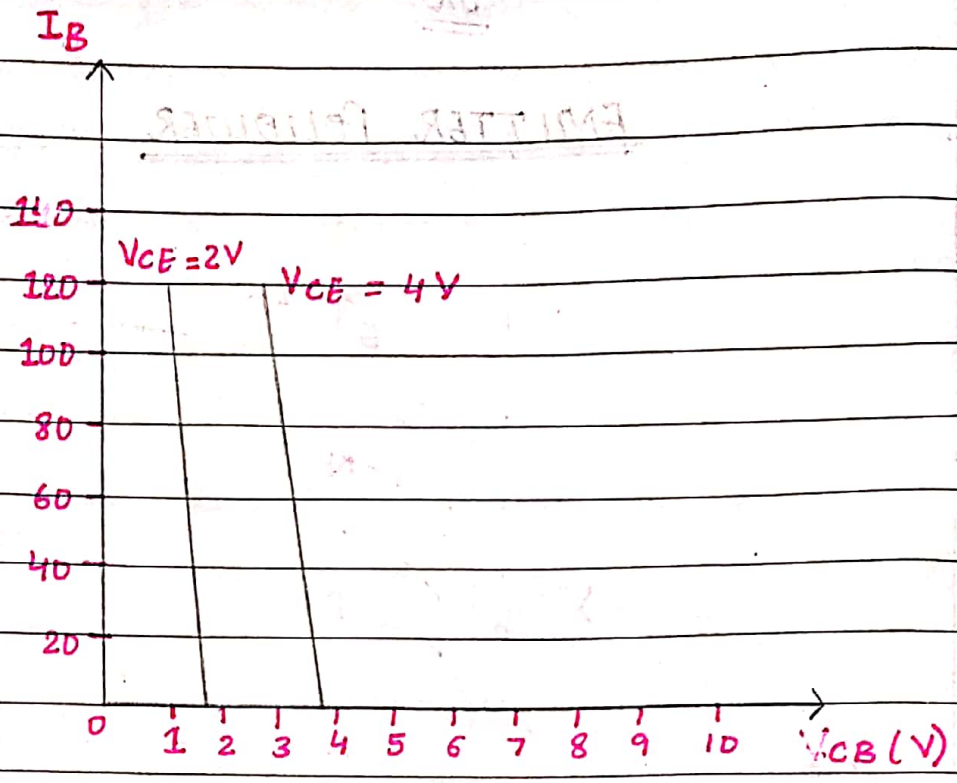
EMITTER FOLLOWER





In common - collector configuration, the collector is common between both input as well as output side as shown in the figure.

- **Input characteristics :**



→ The input characteristics is a graph between input current (I_B) v/s input voltage (V_{CB}).

→ It shows the relation between the input current I_B to the input voltage V_{CB} for the various levels of output voltage V_{CE}.

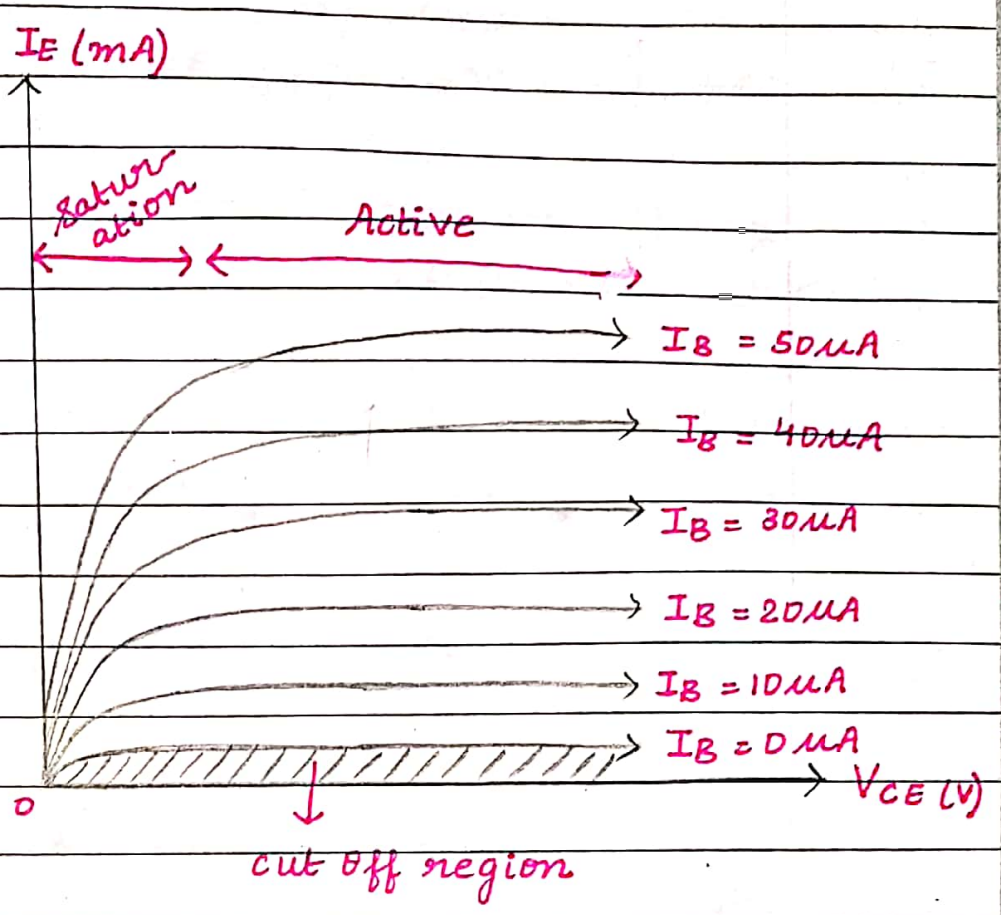
→ It is similar to reverse bias V-I characteristics of a pn-junction diode.

→ When V_{CB} increases, the I_B → base voltage decreases.

→ Dynamic A.C. resistance is given by –

$$r_i = \left.\frac{\Delta V_{CB}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

- **Output Characteristics :**



→ It is the graph between output current (I_E) verses output voltage V_{CE}.

→ It shows the relation between I_E V/s V_{CE} for the various levels of I_B.

→ Dynamic output resistance,

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_E}\right|_{I_B = \text{constant}}$$

- **Active Region :**

Ques Why CE is mostly used as an Amplifier?

⇒ most values are medium/ high/ very high

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Date

*

S.No	Characteristics	CB	CE	CC
1.	Input Impedence/ Resistance	Low (100Ω)	Medium (800Ω)	V-High (750 KΩ)
2.	Output Impedence	Very High (500KΩ)	High (50 KΩ)	Low (50Ω)
3.	Voltage Gain	High (< 150)	Very high (< 500)	low <1
4.	Current Gain	Nearly unity (low)	High (100)	High (100)
5.	Phase Reversal	No	Yes	No
6.	Power Gain	High	High	Low
7.	Applications	Very High Freq. Voltage Amplifier	Audio Freq. power Amplifier	Impedance matching Current Amplifier

⇒ Common emitter circuits are mostly used because its current gain, voltage gain and power gain are quite high and output to input impedence ratio is moderate.

* JFET [Junction Field Effect Transistor] :

⇓

working is same as tap and fan.

⇒ The current flow in JFET is controlled by an electric field set up by an external voltage source is called Field Effect.

⇒ It is an uni-polar device because current flow due to only one type of charges i.e. majority charge carriers.

• Advantages of JFET over BJT :

1) JFET is an uni-polar device whereas BJT is a bi-polar device.

2) It requires less space as compared to BJT.

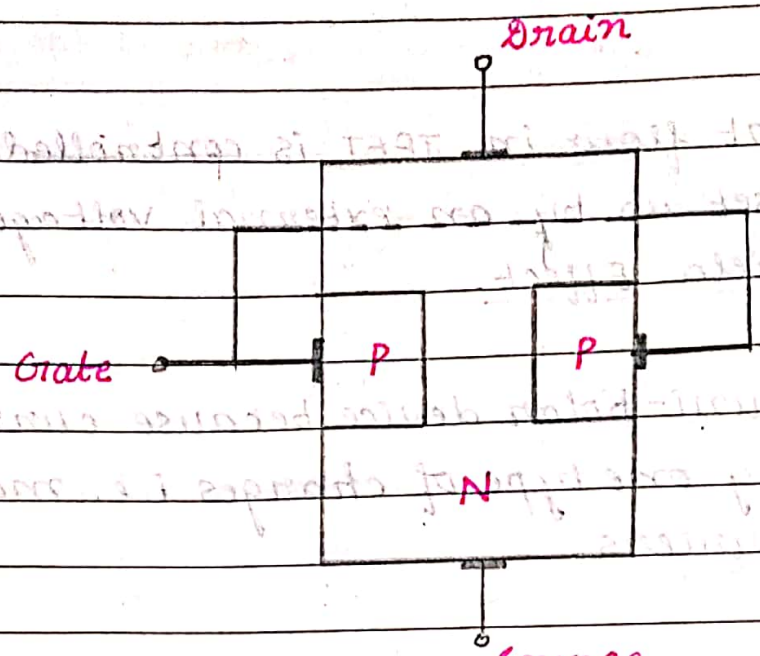
3) It has better thermal stability as compared to BJT.

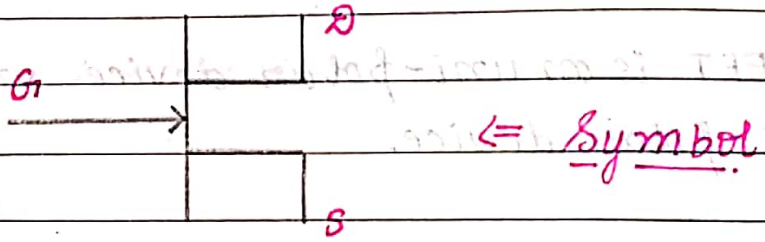
4) It is less affected by noise as compared to BJT.

5) JFET is a voltage-control device whereas BJT is a current-control device.

6) It has high input impedence.

Construction of N-Channel JFET :-





1) A semiconductor material of n-type is taken and ohmic contacts are made at both the ends are called Drain (D) and source (S) terminals of JFET.
2) Both sides of n-type material (left & right side) are heavily doped p-type regions are formed by ~~diffusing~~ diffusion to create p-n junction.
3) N-type material is lightly doped and p-type materials are heavily doped.
4) The thin region between 2 p-type material is called "channel". Since, this channel is created in n-type material, hence, it is called n-channel JFET.
5) Both the p-regions are connected together to form a Gate terminal of JFET.

Date

* ⇒ Working of N-channel JFET :-

1) No bias :

(a) Under no bias condition, that means no external DC source is applied, only depletion regions are formed, no current flows under this condition.

2) $V_{GS} = 0$, V_{DS} is positive :

(a) When we keep $V_{GS} = 0$ and apply positive V_{DS} then, the depletion region is wider near the top of both p-type materials because, the upper region of p-type material is reverse bias and lower region is less reverse bias [approximately forward bias].

(b) Since, the p-n junction is reverse bias, across Gate terminal, resulting gate current becomes zero. [$I_G = 0$] which is the most important characteristics of JFET.

(c) When $V_{GS} = 0$, i.e., no bias but due to V_{DS}, the electrons in the channel will flow from source to drain and current I_D, will flow from drain to source.

(d) As we keep on increasing V_{DS}, the depletion region keeps on increasing and the channel becomes narrow. At a certain voltage, the depletion regions almost touch each other and current becomes constant, is called PINCH OF VOLTAGE.

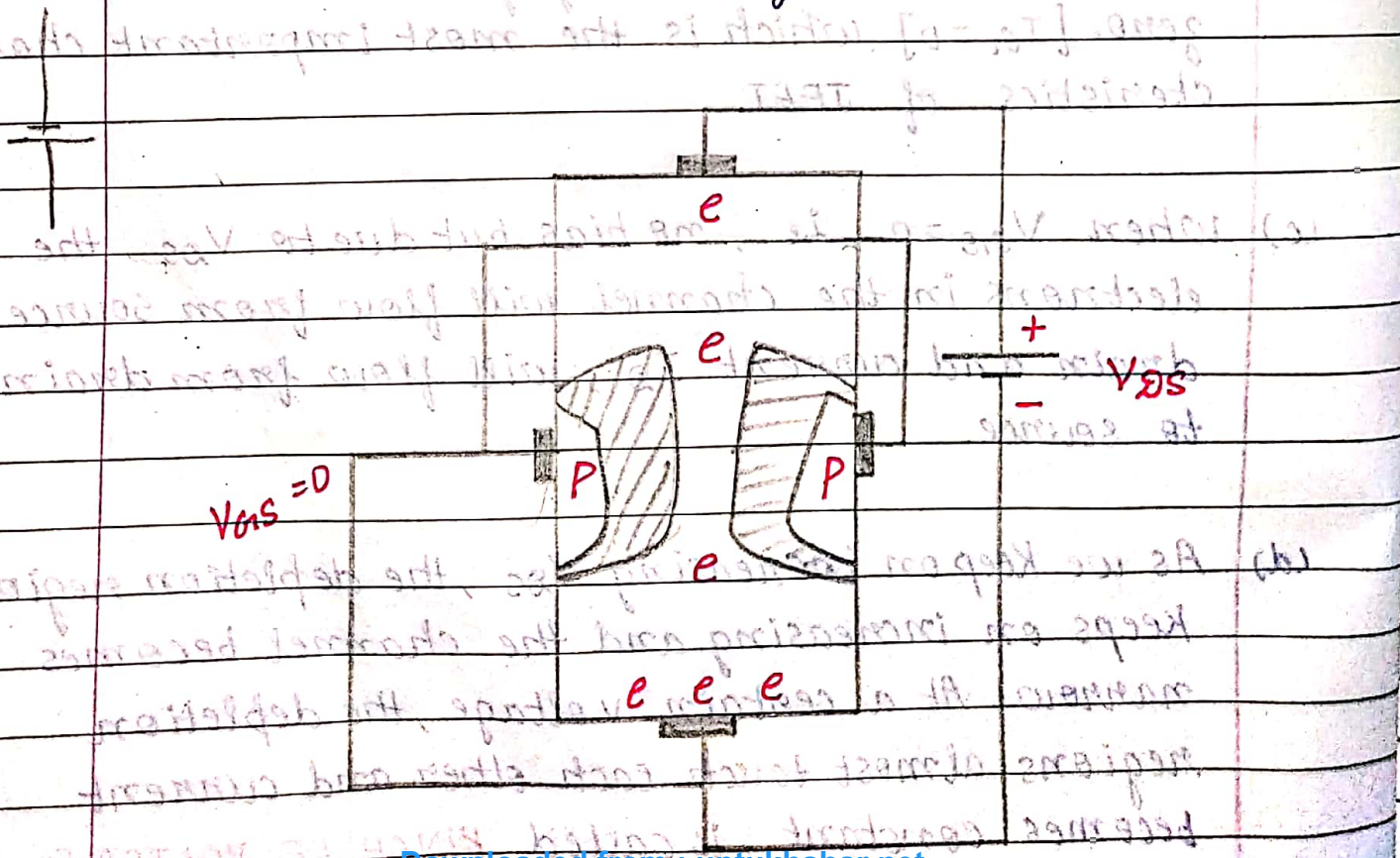
and this condition is called PINCH OF CONDITION.

(c) At the 'pinch of' point any further increase in V_{DS} doesn't produce any increase in I_D, that means, the value of drain current I_D is maximum when $V_{GS} = 0$ and is denoted as I_{DSS}.

3) V_{GS} is small negative, V_{DS} is positive :-

(a) When a small negative voltage is applied between gate and source, due to the reverse bias the penetration of depletion region into the n-type material increases.

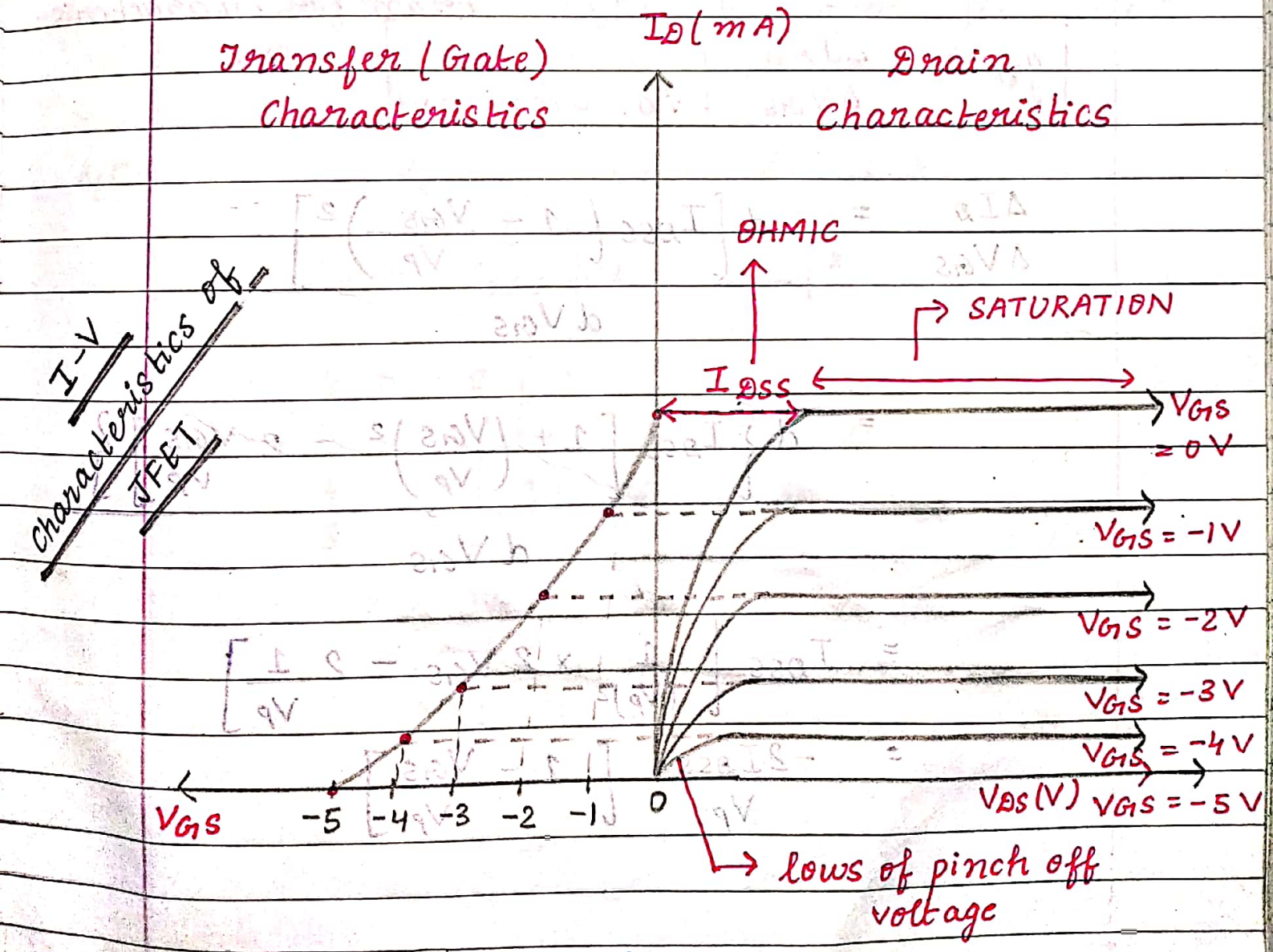
(b) This will reduce the channel width further and due to reduced channel width, less number of electrons can pass through the channel from source to drain and drain current I_D, reduces with the increase in negative V_{GS}.



4) V_{GS} is large negative, V_{DS} is positive :

(a) As negative V_{GS} is further increased, the depletion region penetrates more inside the n-type material. At a certain value of negative V_{GS}, the depletion region touch each other.

(b) The channel width is therefore, becomes zero and the drain current, I_D is also zero. The gate to source voltage at which drain current reduces to zero, is called $V_{GS(off)}$ i.e. $\boxed{V_{GS(off)} = -V_p}$ (not including sign)



* MOSFET (Metal Oxide Semiconductor field effect transistor)

or IGFET (Insulated Gate field effect transistor)

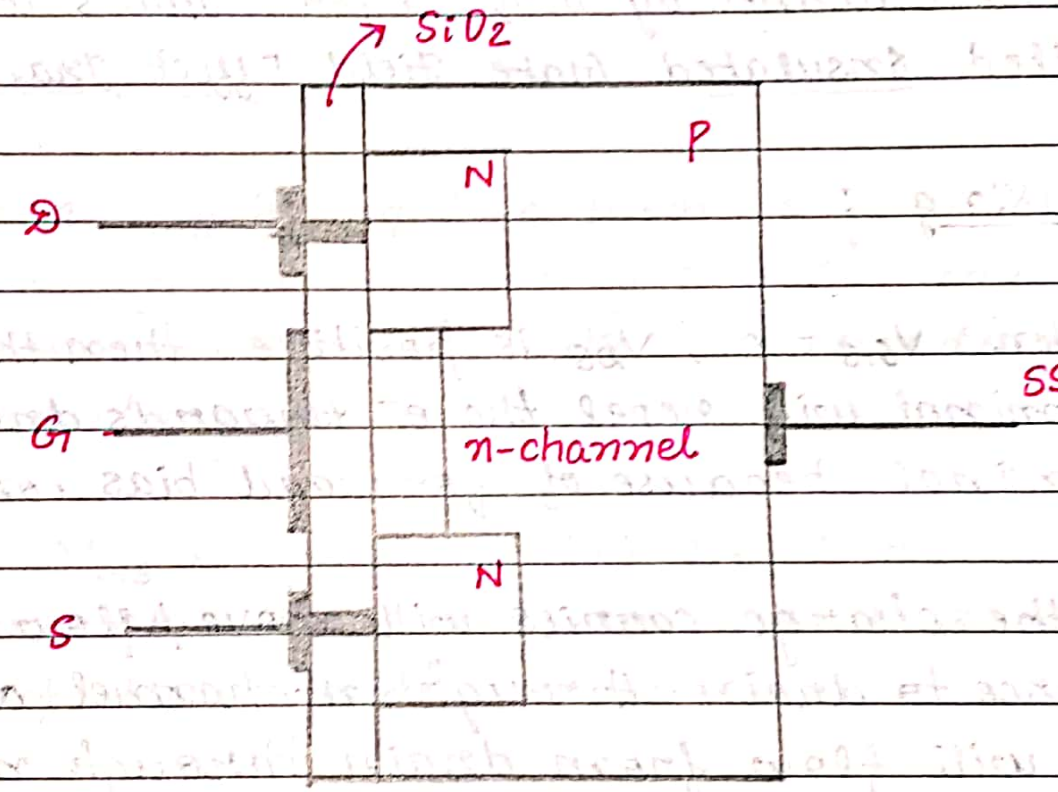
Depletion MOSFET

(i) ⇒ D-MOSFET (n-channel and p-channel)

(ii) ⇒ E-MOSFET (n-channel and p-channel)

Enhancement MOSFET

→ (i) D-MOSFET : (n-channel)



• Construction of n-channel Depletion MOSFET (D-MOSF

1) In n-channel MOSFET, a p-type of semiconductor material is used as a substrate. Usually substrate is connected to a source but sometimes it is taken as a seperate terminal.

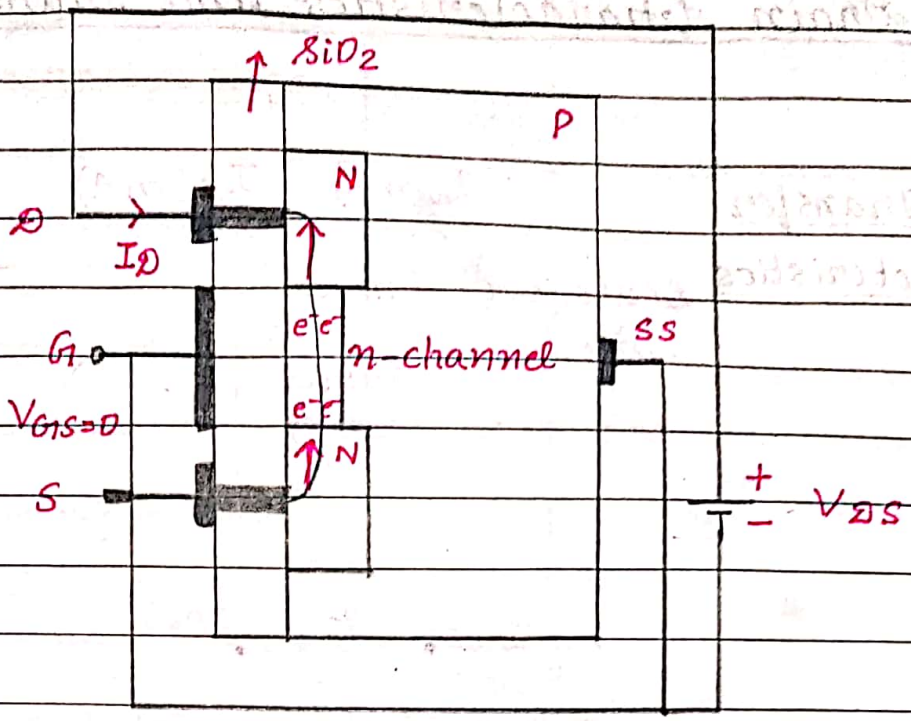
2) Drain and source are connected to n-type regions through metallic contact and they are linked with each other by n-channel. Gate is insulated from channel by SiO_2 layer. That's why it is called Insulated Gate Field Effect Transistor.

• Working :

1.a) When $V_{GS} = 0$, V_{DS} is positive then the source terminal will repel the e^- towards drain terminal because of forward bias condition.

So the charge carries will move / flow from source to drain through n-channel and current will flow from drain to source terminal.

$$V_{GS} = 0 \Rightarrow I_D = I_{DSS}$$

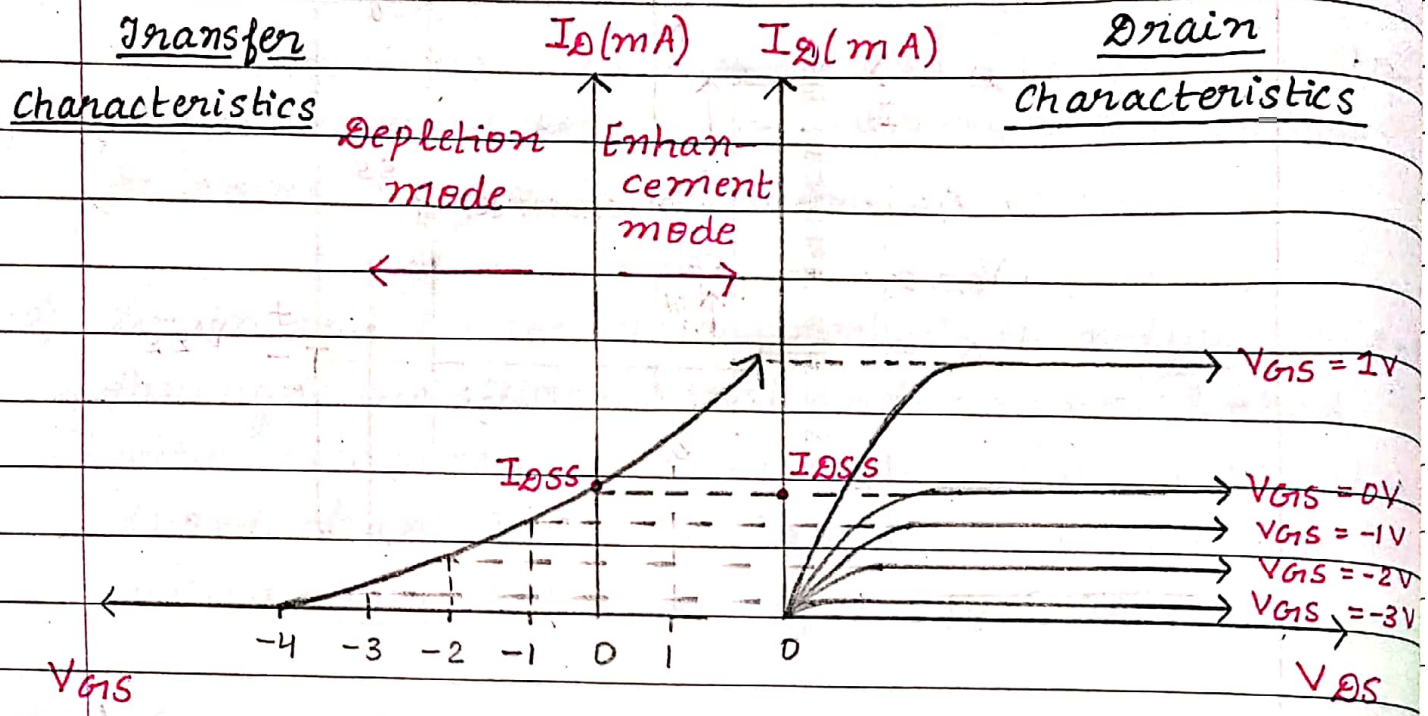


(b) When V_{GS} is negative then e⁻s from n-channel will repelled towards p-type substrate and recombination will take place inside the channel and charge carriers will be reduced.

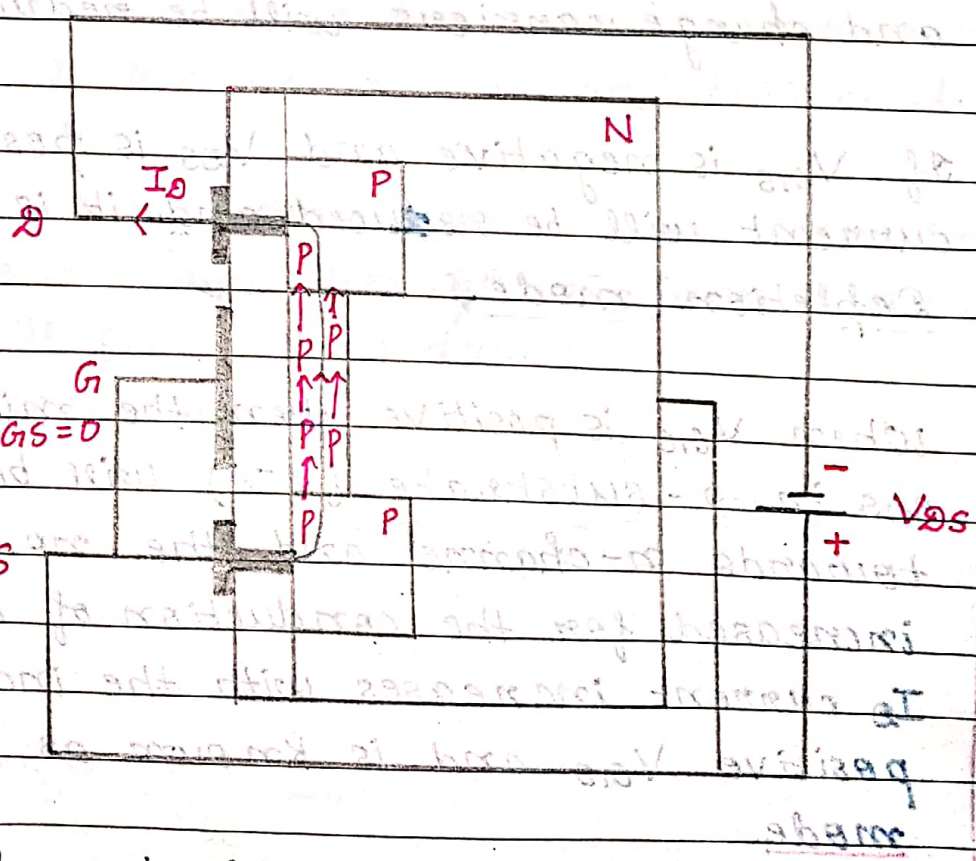
If V_{GS} is negative and V_{DS} is positive the I_D current will be reduced and it is known as Depletion mode.

(c) When V_{GS} is positive then the minority carriers in p-substrate (e⁻s) will be attracted towards n-channel and the no. of e⁻s will be increased for the conduction of current. So, I_D current increases with the increase of positive V_{GS} and is known as Enhancement mode.

- **Drain Characteristics and Transfer Characteristics :**



(ii) ⇒ **p-channel (D - MOSFET) :**



- **VI- Characteristics :**