* March presed upressed # * Introduction to Semiconductons: Semiconductor :-It is a material that has conductivity between Insulator and conductor. Eg - Silicon and Germanium. => bonducton: bonducton is a material which have veny high conductivity because of presence of lange no. of free electrons. Eg-Metal ⇒ Insulaton: It is a material which have almo-St no conductivity because of absence of free electrons. Eg - wood, plastic, paper, etc. > The semiconductors have negative temperature coefficients of nesistance. That means with the increase of temperature, the resistivity of semiconductons decneases. zero Kelvin At absolute zero temperature (i.e. OK), the semiconductors behaves like insulator and it becomes a good conductor at high temperature. At high temperature, the semiconductors behaves like conductors because the valence electrons absorbs Sufficient then mal energy to break the covalent bond and produces free carriers. This increases the no. of carries with increase in conductivity and lowers the resistance. Downloaded from : uptukhabar.net

Mnengy Band Diagnam * Enengy -4-Conduction Band Q. Eg > 5 BY Епегду Вапо Спар Valence Band 4 = Insulatons Enengy Conduction Band Egviev Valence Band Semi bonductors Enengy 5= 112 Conduction Band ZOND ITHE GZONE of overlapping, Eg = 0 1.4.1 1 Valence Band 6 Conductors Downloaded from uptukhabar net

* Jypes of Semiconducton: 1] Intrinsic semiconductor : It is the purest form of Semiconductor without any impunities is called Intrinsic Semiconductor. Eg - Silicon, Genmanium Anna in Sie Sie Sie Sie · calaufaceasir * 20100 4 t= Intrinsic Sami America Semiconducton AL alsoffute 1. all the electron 2] <u>Extrinsic Semiconductor</u> : In this, adding Small amount of impurities in a semiconductor is called Extrinsic semiconductor => The process of adding impurities into a semiconducton is called Doping. In retained trying - There are two types of Extrinsic material based on the impurities added to it, these are -> p-type (Inivalent Impunities) Hivite > n-type (Pentavalent Impunities) exerciteradueton tehover the month conducters Downloaded from : uptukhabar.net

> free electron bside bside = n-type pextna = n-type performance = n-type performantsig tsig (2 Marks Bues) * Effect of Jemperature on Semiconductor: > The electrical conductivity of a semiconductor changes with the variation in temperature. At absolute D(zero) temperature, all the electrons are tightly held by the semiconducton atoms. At this temperature, the covalent bonds are very Strong and there are no free electrons. Therefore, the semiconductor behaves like a <u>perfect Insulator at O (zero) Kelvin.</u> when the temperature is applied across the semi-=> conductor, due to regative (-ve) temp. coefficient, resistivity across the semiconductor decreases and conductivity increases. Hence, at high temp. Semiconductor behaves like a <u>perfect conductor</u>. N-type Semiconductors > * The n-type semiconductons are created by intro- \Rightarrow ducing those type of element which have 5 valen= ce electrons (pentavalent) Such as Phosphonous, Ansenic and Antimony Downloaded from: uptukhabar.net

> N-type contains electrons as majority carriers and few thermally generated minority holes.) although type material is ferraled by depining the se > The process of adding impurity is known as Doping and the material used as impunity in doping process is known as Dopant. > The thing front comprishes represented the presented as => When pentavalent impurities is added to make n-type semiconductors, an additional fifth electron due to the impurity atom remains free. This remaining electrons on free es loosely bound to its parent atom and is relatively free to move within the newly formed n-type in anterial reasons with should trade anterio And this matter definition population hiles => Since, the insented impurity atom has donated a relatively free electron to the structure, this diffused impurities with 5 valence electrons are called Donon atoms => In a: n-type material, the e- is called majority carriers and holes are minority carriers. Donon Deniti carriens (holes) Water and the Atom (positive <u>N-type</u> conniens (electrons) ion as one e-becomes free)

* <u>P-type Semiconductors</u> > ed minerity How we have a start -> The p-type material is formed by doping those types of impunities having 3 valence ets such as Boron, Gallium and Indium (Inivalent). シ The trivalent impurities, consists three (3) e-s in the outermost onbit and it is always ready to accept one e-. Hence, it is called Acceptor Ampunity / ion and all all all Due to three (3) valence e's in Bonon, there is an insufficient number of es to complete the covalent bonds with Silicon and Germanium And, this nesults deficiency of e- called holes represented by small circle on +ve sign. manar the the 18 ho In a p-type material, the holes are majority carriers and es are minority carriers. the or the set person the training to the to $\frac{+++--+}{+++-}$ $\frac{-++++-}{+++-+}$ $\frac{Minomity}{t} + \frac{+++-+}{t}$ $\frac{-++++--+}{t}$ $\frac{-++++--+}{t}$ $\frac{-++++--+}{t}$ + + Majonity
 canniens (holes) Accepton Impurity / Son

Pn-Junction Diode on Semiconductor Diode :-=> pand n-type of Semiconductors combine together by means of some physical process which do not disturb the crystalline structure is known as <u>pn-junction Diede</u>. P No Bias condition : In this condition, p and n-types of materials are combined and no external supply is given (DC). caidagenta 1/- 9 · p-type materials contains holes as majority carriers and n-type materials have electrons as majority carriers. Hence, there is a concert nation difference of changes. · Due to the concentration difference, holes from 'p' side to 'n' side and electrons from 'n' side to 'p' side starts flowing (from high conc. area to low conc. area). This process is called Diffusion • As holes crosses the junction from 'p' to 'n' and electrons crossess the junction from 'n' to 'p', So there will be recombination of charges because of which holes will be necombine with free electnons and electrons with tiples · Because of recombination the accepton ion on 'p side and donor ion on 'n' side will be collected accross the junction on near the junction primerat av- and done had not These -ve changes on p' side and +ve changes on _____n' side across the junction will form a layer which is called Depletion layer.

Immobile Ions a e-(majonity carriers) n -holes-+ + -GOIDT + (majority carriers) + - + OO DO + 0 +- @- $\Theta \Theta \oplus \oplus$ ++++ - @ a Donon ions +++++ OO DA $\oplus - \oplus -$ OODD +0++-Accepton & OODO + holes (minoning conviens) ナナナナキ ion - 4 - + - + e-E (minonity Depletion carriers) layer P-N Junction The region where there is no mobile charges, only Immobile on fixed changes are available is known as Depletion region, due to fixed ions which are electrically charged it is also known as Space change region when the pn-junction is created there is no movement of electrons and holes stops because it electnons and holes will be repelled due to the layer of -ve immobile ions and the immobile ions. ¢ Forward Biasing: · when p-type material is connected with +ve terminal of the battery and n-type is connected with the -ve terminal of the battery is called forward Bias. The process of applying external DC Supply Downloaded from : uptukhabar.net is known as Biasing.

Due to the presence of the and we ions across the junction, an electric field is created which is called Barrier potential on Junction Potential on Cut-in voltage. Because of +ve supply at p-terminal, holes will be Repelled towards the junction and due to -ve Supply, es will be Repelled towards the junction of n-tenninal. The holes start neutrilizing the -ve ion of p-side and e-s of n-side. As a result, the depletion layen's width gets reduced. · Pesitive terminal · when the applied forward bias voltage is furthur increased, the depletion layer width will continue formed to decrease until the flow of e- can pass through the junction nesulting in exponential rise in current in forward bias region. magice derivered and specific and flow the + + + - + + + - d+ + 20 Hitring Asides at sub inter Reduced strand apid Depletion wight to subse the jugation

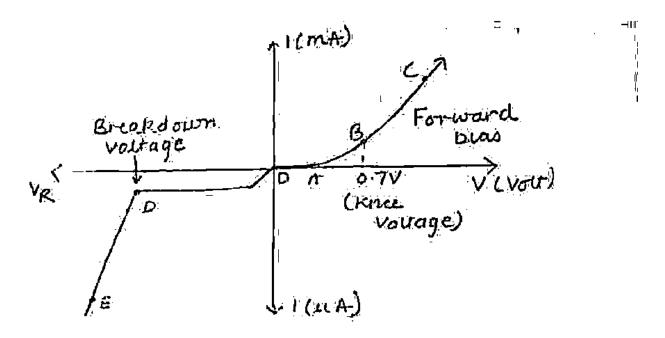
Elle to the parsence of the CAM I- Ve LODIS ac 1955 228) a property (A) with another for the second of the sec · abie factor strigt angutarelising the -ve can of p-side Bar Revense Biasing Positive terminal of the battery is connected with n'side and negative terminal of the battery is connected with p' side is called In Reverse Biasing, holes of the p-negion attracted towards -ve terminal, means away from the function. Similarly, c- will also move towards the tve terminal of the junction. Due to this the depletion region width gets Due to this increased both side of the junction. • This increased depletion layer will also give high barnier potential due to which holes and es from p-side to n-side will be enable to cnoss the junction. · The current flow due to majority charge carriers in neverse bias condition is zero (o) but there. Downloaded from : uptukhabar.net

will be small amount of current (MA for the and mA for Si) will flow due to minority charge carrier. P n CODGOD + 677 W ÷ + + + -OBODAD -7-(-) (-)4 uf: Increases depletion width 7 600920 I(MA) Bneakdown voltage Y N(volt) I (MA)

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I(MA)					
V-I Characteristics of pn-Junction					
Diede					

VI maracteristics of PN Junction Diode

- · Voltage Ampire (V-I) characteristics of PN junction or semiconductor diode is the unite between voltage across the junction and the surrent through the circuit
- . The manacteristics can be explained under three cases such as
 - Zero bias
 - Forward bias
 - Reverse blas
- (1) zoro bias-
 - . In this condition, no external voltage is applied to the p-n junction i.e the circuit is opin. Hence the potential bartiers does not purmit current flow
- · Thurefore, the circuit writent is zero at V=0V, as indicated by point o



(2) Forward bias

- In forward bias condition, p type of pr junction is connected to the positive terminal and n type is connected to nightive terminal of external voltage This results in reduced potential barrier
- From forward characteristics, it can be noted that at first i.e region OA, the wirrord increases very slowly and worke is non which is because in this region the external voltage applied to the pri junction is used in overeming potential barrier.
- At some forward valtage the 0.7V for St & 0.3V for Ge, the potential barrier is almost eliminated and the urrent starts flowing in the circuit
- · From this instant, the unpert increases with the increase in forward voltage. Hence a worke AB is obtained to forward beas
- · However, once the external voltage exceeds the potential barrier voltage. The potential barrier

is eliminated and the projunction behaves as an ordinary conductor. Hence, the curve BC rises very sharply with the increase in external college and the curve is almost linear.

 $\simeq 1$

(3.) Reverse Bias

• An reverse bias condition, the p-type of the pn junction is connected to the nigative terminal and n type of pn junction d'ode is connected to the positive terminal of he external a voltage this results in increased potential barrier at the junction.

· Hence the junction resistance becomes very high and as a result ideally no current flows through the circuit

- However, a very small verrent of the order of u.A. (micro Ampure) Hows through the virait.

 This is known as reverse saturation wrrent(Is)

 This is known as neverse saturation wrrent(Is)
 and it is due to minority varriers in the
 junction shown by OD wrree
- The reverse bias applied to the p-n junction act as forward bias to their minority corrects and hence small current flows in nevern direction
- If reverse voltage is increased by ond particular value, large reverse current can flow damaging the diod. This "called reverse breakdown of a diode represented by DE region in V-I graph.

DIDDE CURRENT EQUATIONS :-* $I = I_{0} = I_{F} = I_{S} e^{V/NV_{T}} -$ I = diode forward current = Ip = Ip 3 Is = Io = TR = Revense Saturation current / Diode Reverse current Vo = VF = V = Divde Forward voltage n = coefficient) = 1 fon Germanium (Ge) = 2 for Silicon (si) <u>KT</u> 9, $V_T =$ 7 $K = Bott_2 man's constant = 1.38 \times 10^{-23} J/K$ T = Jemperature in Kelvin 9 = 1.6 × 10 -19 coulomb

*	IDEAL VS PRACTICAL DIDDE :	si per estas Altre de la constante de la const Altre de la constante de la const
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* of resistance is not given than voltage is o(zero) when cincuit is short, voltage is o when cincuit Page No. is open then voltage is maximum. Date (a) • The nesistance offered by a pn-junction diode when applied voltage is SC then it is known Oc on Static resistance It is denoted by RD and given by the natio of Vo and Is in forward bias condition $V_{\mathcal{F}}$ VØ IØ Rg= IF TO VD VRC RD = VD In IR (b) • Dynamic on Ac nesistance -The nesistance offered by a pn-junction diode when applied vollage is Ac then Known as 15 AC on Dynamic resistance It is denoted by no and is given by the natio AVd and Vmax and i mira 2 inale da 1 IA A VO no = DI8 Vmin atta ar Sa 1 merson Pitik Di Downloaded from : uptukhabar.net

Mathematically it is given as -Mp = JVD JID AD = 1 OID 2VD $\frac{n_{D}}{\frac{\partial}{\partial v_{D}}} = \frac{1}{\frac{1}{2}}$ $\frac{\pi \vartheta}{I_{ge}} = \frac{1}{\frac{V_{\vartheta}}{\eta_{v_T}} \times 1}$ $\frac{1}{\eta_{v_T}}$ $\frac{n_{D}}{I_{S}} = \frac{N_{T}}{I_{S}} = \frac{N_{T}}{I_{D}} = \frac{N_{T}}{I_{D}}$ * DIDDE CAPACITANCE : (a) Diffusion bapacitance (co) (6) Inansmission Capacitance (CT) (a) · Diffusion Capacitance -The capacitance exist in forward bias condition is called <u>Diffusion capacitance on Storage</u> <u>capacitance</u>. • In forward bias condition the width of depletion region decreases and holes from p-side gets diffused into n-side whereas ets from n-p side · As the applied voltage increases, the conc. of charge carrier diffusion also increases. This rate Downloaded from : uptukhabar.net

of change of injected change with applied voltage is defined as capacitance called Diffusion Capacitan $C_{\mathcal{D}} = dR$ dV $\frac{C_{\mathcal{D}} = \mathcal{T}I}{\eta v_{\tau}}$ where t is mean lifetime of fioles. BUNGTORESIDAL CREDITANCE (b) • Inansition capacitance when a diode is in neverse bias, the width of depletion negion increases and there are more no of +ve and -ve charges present in it. • Due to this, the p-region and n-region acts like the flates of capacitance and the widened depletion negion acts like dielectric. · Hence, the existance of capacitance in nevense bias of pn-junction is known as Inansition Capacition on Junction Capacitance or <u>Space change capacitance en Barnien capacitance</u> on Depletion capacitance. Downloaded from uptukhabar.net

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* DIDDE CLIPPERS: (Application of Diode) · An electronic cincuit which used to shape up the waveform on clip off on remove the portion of waveform without distonting the remaining part on portion of the system is known as Diode clipper / Diode clippen cincuit. • It consists of only diode and nesistance. • The input is always given in the form of alternating cycle. → Jypes of <u>Clippens</u> Blippens Case a: 12 Von 20 (20 sitive tradition all Unbiased Biased Combinational in listed will be approved in Mills it acts as arrivers sincerity Series = Parallel/and Judtin with Shunt -ve +ve -ve series Parallel/ +ve Shunt the second secon +ve -ve +ve -ve Downloaded from : uptukhabar.net

Unbiased Series clippen: (Positive) (1). Unbiased=> There is no external OC supply given to the Sincuit and all avances and the set => It will clip off on nemove the complete half cycle of the input waveform. senies \Rightarrow The diode is connected in senies with the load. +ve > Unbiased Series Clipper (positive): If the tve half cycle of the input waveform is removed in the output is known as positive clipper VA o T/2 J RL VO case 1: (i) Vin > 0 (positive half cycle) (Diode (ii) Diode will be nevensed bias (VA iii) it acts as an open circuit. liv) output across RL, Vo = D Vin o T/2 R_L Vo Downloaded from : uptukhabar.net

Case 2: (i) Vin < 0 (negative half cycle) Diode (ii) Diode will be forward biased. VA (iii) It acts as short circuit. (iv) output across load resistance, Vo=Vin ⇒-Vin-IR=0 T/2 & Input \$ RL & VO in 0 >-Vin-(Vo)=0 => Vin=Vo CA80-2 Output > 0 7/2 Unbiased Shunt Negative clippen (2) . an n-littly ------T/2 Vo Vin of 3RL parallel => The diode is connected in parallel with the load nesistance. >> The -ve half cycle of the input waveform is -ve removed in the output is known as negative clippen. Downloaded from : uptukhabar.net

Case 1: RL · T/2 Vin Yp_ Case 1 7 > Vin 70 Vin - IR - Vo =D) Diede becomes > Vo = Vin - IR neversed bias and if RICRL open cincuit. => Vo = Vin > Vo = Vin R Case 2 : Vin P RL Yp $V_o - D = 0$ => Vo=0 " In 11el, the voltage remains same, if one voltage is short I.e. 0 (zero) then the other will also be D(zero) i.e. Vo = D. Case 2 => > Vin < D > Diode becomes forward beas and short cincul Output = o T/2 > Vo= D. (3) · Unbiased series negative clipper. 14) . Unbiased shunt positive clipper Downloaded from : uptukhabar.net

15) BIASED CLIPPER Vo - ----Vin. D + VR Case 1: (i) Vin > VR ii, Diode becomes fonward bias. (iii) It behaves like a short cincuit (iv) Apply KVL to get output. 11) Batterny (Amoon chieve to up or workicher Kiele reas to the second stabil and it about its A MARCH WIR 6-2-Vo a contract is Vin <u>|+</u> _{VR} T-181188 111 $V_{in} - V_o = O \qquad \begin{cases} y'' & V_{in} - IR - V_R = O \end{cases}$ ⇒ Vin = Vo. remains the same. Case2: (i) Vin (VR in Diode becomes neversed bias (iii) It behaves like an open cincuit iv, Apply KVL to get output Vin Downloaded from : uptukhabar.net-

VR - IR = Vo: RAGATIO RAZAIR (3) \rightarrow $V_R = V_D$ (IR=D : I=D : open cincuit Butput :-Vin VR here must france & chear ⋇ Direct Method: time Annual Man Man ask enternal (1) Battery (from down to up on anticlockwise) 12) Diode I from the nearest node, 1st sign ⇒ if +ve upper pontion is removed =) if -ve lower portion is removed) <u>Bues</u> (i) Vin (ii) 0 Vindo Ye adia the -Anni. (iii) Vo Vin. Downloaded from : uptukhabar.net

+10 ij Ans I/P ... 0 - 10 + 10. D/P D -10 -CIPPER * AMAITAMAN +10. in 5 IP 0 -10 . +10 0 D/P -10. 10 (iii) -10 I/P 10 Q * In same polarity of diode & battery 5 DP -10 . then add otherwise solve using KVL. Gie ~ Rues (i) 0.3Y 7. 2.7 31 -7 (ii) 10 Si 0.7V 10 Δ 5.7 57 -12 -12 5 1× Downloaded from : uptukhabar.net

iii -、 10 si 0.7V 5 V -4.3 -10 ID ¥ OMBINATIONAL CLIPPER :-* solve both + of them seperated and then give 10 -10 5V51 the final otitput. 10 E output 5 -5 -10 31 Ques +10 7 +10+ +-3 シ Vo -10-10 7 シ D/F 0 e i i i Downloaded from : uptukhabar.net

5vaues i (4) +10 Vin -5 -10 6 -5 410 15 5vii) -10 32 Vin 15 D/P . heel b -dite the SL (I)D 10-0.7 10 3.7 O/P ø 6 D gier A 4 -15 3V 15 JHPES OF CLAMPER ÷ (2) 10 10 0.3 Gie -2.7 -10 o/P Yo 0 31 -10 1 Gie 51 O/P -5.3 10 (3) ravi L X J 10 - 10 10 OA D 4.7 -10 Downloaded from : uptukhabar.net

Î Ve 10---15 -3 * <u>CLAMPER CIRCUIT: - [Application of Diode</u>) clampen is an electronic cincuit that is constructed using a capaciton, a diode and load nesiston that shifts the wave form to a different level without changing the appearance of applied signal. blampen does not change the shape of the wave-forms and feak to feak value. JYPES OF CLAMPER :-• Clampen Biased Unbiased +ve--ve +ve (positive) (negative) (positive) (negative) Downloaded from : uptukhabar.net

Unbiased Positive clampen :- (Direct Method) 1) * See where the sharpness side of the arrow is that side Vo only the whole -10 + Montput will shift. => Hene, upwards 20 Dinect D/P Method 20 2) Unbiased Negative clamper :- (Dinect Method) 10 -15 CIAND: D ¥. UNRIAGES 10 0 -10 -15 - 20 -25 3) Biased Pasitive clampen :- (Dinect Method) Planner 1 4 sunsoin Apple 1 L SV -10 Downloaded from : uptukhabar.net

15 Martine Restricter and ALAIM fè TD 5 0/P -5 (e e): -10 Biased Negative clamper :- (Direct Method) 4] 5V _____ 10 1 nam haspiter -4.31 D/P ------>E * UNBLASED CLAMPER + Note: 1) Start with cycle which makes divide short cincuit (forward bias) (2) Apply KV2 for the half cycle in 1st loop. -consider => > Vin-Ve = 0 (+ve cycle sign of Vn (inner loop) Downloaded from : uptukhabar.net

RUCS = $V_c = V_{in}$ Consider sign of Vin = -Vin + Vo = 0 => Vo = Vin (-ve cycle inner loop) don't .=> Vin-Ve-Vo = D (+ve cycle outer sign of Vin then > Vo = Vin - Vc - 0 loop) afterwards take the sign seperately. For the cycle -Vo = Vin - Vc = Vin - Vin > Vo=D JVX preinto Th For -ve cycle -- -ve --- $V_o = -V_{in} - V_c = -V_{in} - V_{in}^{-2V_{in}}$ => Vo = -2 Vin At axis > Vo = -Ve • > Vin + Vc + Vo = DV -1 $\Rightarrow \quad \forall o: = + \forall in + \forall c - 2$ Fon the cycle - Vo = Vin + VG = Vin + Vin \Rightarrow $V_0 = 2V_{in}$ FOR THE FOUL PULLER A Fon -ve cycle ----Vo = - Vin + Vc = - Vin + Vin $\Rightarrow [V_0 = 0]$ At anis => Vo = Vc Vc Var = - Vinal - Va WE FUT - VI Downloaded from . uptukhabar.net

+11-Ques 7 . 3V Yo + ··· Vie V tim +600 1 Vin 1 2 Vow to post -31-Applying KVL, -linnen loop) Vin - Ve --- , 3 = D $Vin - V_c = 3$ Vin (max) = 10 $\Rightarrow 10 - V_c = 3 \Rightarrow V_c = 7V$ ()---- () an 2 - 2 - 2 - 2 Applying KVL, (outer loop) $V_{in} - V_e - V_o = D$ Vo = Vin -Vc - D For + ve half cycle -> Vo = Vin - Vc and + = ...10 - 7. V = 3= ... = $V_0 = 3V$ Fon the half cycle -> $V_o = -V_{in} - V_c$ = -10 - 7 = -17 $V_0 = -17V$ For axis, $V_0 = 0 - 7 = -7V$

AMADIA output -3. -7 ---Bues Vin 7 7 Applying KVL (inner), $-V_{in} + V_c - 3 = 0$ way Try Cast AC = 3 (worki) Iny busing the $V_{c} = V_{in} + 3 = +10 + 3 = -3V$ Will an I and a will a Applying KVL (outer), Wall = + Vin + VG - Vo = D $\left[V_{o} = + V_{in} + V_{c}\right] = 0$ (Fine For the half cycle sal in printing 0 = V- V+ Vo = Vin + Ve = 10-+13 = 231V for ve half cycles ind we wat $V_0 = +03V - 01$ At anis, Vin =0 VIII = - M Vo = Vin + Ve = 0+13 = +13V

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air and the Bues ZRL VO 1D Ame 34 VC 0.3 Vin 37 Applying KVL (inner), $-V_{in} + V_c + v.3 - 3 = 0$ $-10 + V_{c} - 2.7 = 0$ VG = 12.7 V Applying KVL (outer), $V_{in} + V_G - V_O = D$ $V_0 = V_{in} + V_c - 0$ For the half cycle, $V_0 = 10 + 12.7$ Vo = 22.7V Fon -ve half cycle, $V_0 = -10 + 12.7$ $V_0 = 2.7V$

At (anis) Vincenterent - 283191103 × => Vo = VG = 12.7 V :5 Hall wave Receil 22.7 -12.7 --> = output 2.7 0 + + Bues + D.7V 2 RL Si Vin 31 36 8 6 6 6 M Applying KVL (inner), $V_{in} - V_c - 0.7 + 3 = 0$ $10 - V_{c} - 0.7 + 3 = 0$ $V_{c} = 12.3V$ Applying KVL (outer), _____ $V_{in} - V_c - V_0 = 0$ \Rightarrow $V_0 = Vin - V_c - O$ Fon the cycle, => Vo = 10 - 12.3 => Vo = -2.3V For -ve cycle, => Vo = -10 - 12.3 > Vo = -22.3V At axis, Vin = 2 $V_{2} = 2 - 12 \cdot 3 = V_{2} = -10 \cdot 3 v$ ante in dial Search 18138 and Stands 101 E output - 2.3 -10.3 ---->+ - 22.3 -Downloaded from : uptukhabar.net

* KECTIFIERS :- (Application of Diode) 5.81 = V = V 5 Half wave Rectifier: * 1) l= Butput ₽ RL (AC) YD 23110 Description of the circuit - \Rightarrow · Half wave Rectifier consists of atransformer, a diode and resistive load in we proming the It provides the output for only half cycle of the input waveformer a - al => working - $V = V = V_0 = 0$ (a) <u>Positive Half bycle</u>: M 5.<u>C</u>. 10100 +211-T - Ve clicte 6 5.91-In the half cycle of A.C. input, the diade will • openate in forward bias and starts conducting. Eulpul

· In this interval, the diode gives the output in the same phase applied as input A.C. voltage as shown in the figure. 16) Negative Half bycle: 0.6. ÎÎ 2ÎÎ Vin. 21 2 RL Vo ÷ In -ve half cycle the polarity of the applied voltage is neversed and due to this the diade will become nevensed biased and do not conduct i.e. open cincuit. The output across the load resistance Ry will be o(zero). because of nevense biasing of the diode. Input, output waveform -=> Î 211 I/P - 0-411 DPE 311 211 Downloaded from : uptukhabar.net

* 1) OC on Avenage Load Gurrent (Ioc on IAvg): IDC BA Javg = 1 jind(wt) iz = Imsinwt $\Rightarrow I_{avg} = \frac{1}{2\pi} \int_{0}^{\pi} I_{m} sin wt d(wt) + \int_{0}^{\pi} d(wt) \\ \overline{n}$ $= \frac{Im}{2\pi} \left[-\cos \omega t \right]_{0}^{\pi}$ $= \frac{\mathrm{Im}}{2\pi} \left[-(-1) - (-1) \right]$ <u>= Im x 2</u> 211 IDC OR Iarg = Im RMS load current (________; 2)* E- $\begin{bmatrix} 2\pi \\ j & i^2 \\ 2\pi \\ z \end{bmatrix} = \begin{bmatrix} 2\pi \\ j \\ z \end{bmatrix} \begin{bmatrix} 2\pi \\ z \end{bmatrix} = \begin{bmatrix} 2\pi \\ z \end{bmatrix}$ Inms = $= \begin{bmatrix} 1 & \int Im^2 \sin^2 \omega t \, d(\omega t) \end{bmatrix}$ 1/2 $= \frac{\mathrm{Im}^{2} \left(\left(1 - \cos 2 \omega t \right) d \left(\omega t \right) \right)}{4 \pi}$ Downloaded from . uptukhabar.net

 $\frac{Im^2}{4\pi} \int tot = stn 2wt \int \pi$ CONTRACTOR EGITOR $Im^2 \left[\widehat{\Pi} - sin \widehat{\Pi} - o - o \right]$ -2 $\frac{\mathrm{Im}^2 \times \overline{\mathcal{M}}}{4\overline{\mathcal{M}}}$ 1 Im <u>Im</u> 2 3) * Ripple jacton : (n) · It is defined as the percentage of AC content present in the output, it's ideal value should be Olzero) and the practical should be as low as possible. · Mathematically, it is expressed as $\frac{I_{nms}^{2} = I_{AC}^{2} + I_{DC}^{2}}{I_{AC}^{2} + I_{DC}^{2}}$ · Y= Rimis value of Aic Component of O/P (I Ac)nms Inms 2 - I BC 2 = JAC2 Inc on (Inc)nms - Inms - Toc Dc Component of ofp Inms² - IDC² 91, = Ipc 2 $\frac{|I_{nms}|^2 - 1}{|I_{DC}|}$ Im^2 91. = 2×2 - 1 Im² TXI Downloaded from : uptukhabar.net

n + ++++ = = 1.21 4) * Rectification Efficiency: • It is defined as the natio of output DC power to the AC input power. · Mathematically, it can be expressed as - $\frac{1}{2}\frac{\eta}{\eta} = \frac{P_{ODC} \times 100}{P_{IAC}}$ $\frac{3}{\sqrt{2}} \frac{\gamma}{2} = \frac{I_{dc} \times R}{I_{dc} \times R} = \frac{I_{m}}{1} \frac{2}{1} \times 100$ situa 10 to sport part of Balilion pice is and it is the X 10 Ding add at = 40.53 % => / n = 40.53 % 5) * Average on DC voltage: Rs > winding VOC = IDC X RL nesistance Rf > forward VDC = Im X RL resistance of diode Ex So $= Vm \Rightarrow V_{DC} = Vm$ 5.7 A K F Downloaded from : uptukhabar.net

6) Peak Inverse Voltage (PIV): > The peak Inverse voltage is the peak voltage across the diode in the reverse direction; i.e. when diode is reverse bias condition, Called PIV rating of a dide. -> In half wave rectifier, the load current is ideally zero when the diode is reverse biased and hence the maximum value of the vottage that Con enist Across the diode is Vm. PIV = Mm PIV = Vm for Half wave rectifier (7) Transformer Utilization Factor (T.U.F.) -> The T.U.F. is defined as the vatio of D.C. power delivered to the load to the A.C. power rating of the transformer. T.U.F. = D.C. power delivered to the load A.C. power rating of the Transformer PDC -> for half wave rectifier . T.U.F. = PRMS $\rightarrow P_{DC} = I_{DC}^2 \times R_L = (I_m)^2 \times R_L$ -> AC power Rating of transformer = VRMS. JRMS -> Mmx Im JE 2 = InRLKIM 77 192 KG $\frac{1}{12} \frac{2\sqrt{2}}{12} \frac{2\sqrt{2}}{12} = 0.287$ $\frac{1}{2\sqrt{2}} \frac{2\sqrt{2}}{12} = 0.287$ $\frac{1}{2\sqrt{2}} \frac{2\sqrt{2}}{2\sqrt{2}}$ T.D.F = almost a your of a falling T.U.F. = 0.287 01 x 1 ...

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(8) Voltage Regulation (VTC) aprilia -> The voltage regulation is the factor which tells us about the change in the d.c. output voltage as load changes from no load to full load condition. -> if (Vdc) AL = D.C. Voltage on NO Lord (Vdc)FL = D.C. voltage on full load then voltage regulation is defined as 1. Voltage Regulation(R)= (Vac)ril - (Vac)FL X 10D -> for half wave (Vac)an = Vm (Vdc)FL = IDCXRL = In XRL IT TI (RITRARS) TI TI (RL+RFRS) XRL : 10 R = Vm d RL Tr (Retlepths) - RL TRITRETRS) RithgtRs-Bt Ritty th) RL+Rg+Rs) RL (Billythy) :. 1. R = (Rg+Rs) × 100 regtating secondary winding 1% R = R X 100 Downloaded from : uptukhabar.net

AC on RMS load voltage : E) * Vams = Iams X RL Vorms = Im XRL $= \frac{\sqrt{m}}{2(R_L + R_S + R_g)} \times R_L \quad \{R_L \cong R_S + R_f + R_L\}$ = Vm=> Verms = Vm Full wave Rectifien: 2) . V. V. V. Omp (i) GENTRE TAPPED RECTIFIER ହା H allins h RL E-Vo-> D2 \Rightarrow Description of the cincuit -· bentre tapped rectifien consists of a centre-tapped transformer, two diodes and presistive load. Downloaded from : uptukhabar.net

It gives output for both cycle. -> Working has <u>Positive Half by cle</u>: \mathcal{D}_{l} Vin DI E+ EV0-> During the half cycle, the applied voltage is passed through the step-down transformer (centre tapped) and diode D, operates in forward bias and D2 openates in reversed bias. The output across the load resistance RL will be in the same phase with input due to diode of as shown in figure. (b) Negative Half by cle F E+ -V0-> 1 21 Vin + D2 million the former + • In negative half cycle the polarity will be nevensed, Diode D, operates in nevensed bias Downloaded from : uptukhabar.net

and divde De in forward bias The output across the load resistance will be 180° outer phase with the input due to Diode D2 and properties of centre tapper transformer. Input, output waveform - \Rightarrow this (the mix of 211 ITS D/P < T 211 DC on Avenage Load current (Ipc or Tavg) 1)* $\frac{I_{DC} = \frac{1}{2\pi} \int_{-\infty}^{\infty} i_{L} d(wt)$ 2 The phas = 1 [Jmsinwt d(wt) + JO Imsinwt d(wt) $= \operatorname{Im} \left[\left[-\frac{1}{2\pi} \cos \omega t \right]_{D}^{\overline{n}} + \left[\cos \omega t \right]_{\overline{n}}^{2\overline{n}} \right]$ $= 2\overline{n} \left[\left[-\frac{1}{2\pi} \cos \omega t \right]_{D}^{\overline{n}} + \left[\cos \omega t \right]_{\overline{n}}^{2\overline{n}} \right]$ $\frac{-1}{2\pi} = \frac{1}{2\pi} \left[\frac{-(-1)+1}{-(-1)} - \frac{-(-1)+(-1)}{-(-1)} \right]$ $= Im \times 4^2$ $1 2\pi$ STRI 1/2 $a_{11,0} = 2Im$ Downloaded from : uptukhabar.net

2Im T nh n Inc on Tav = IAG ON Inms * square 2) AC RMS noot On mean 21 1/2 $\frac{1}{2}d(wt)$ Inms = 217 1/2 . 21) takenrone $n^2 w t$) d(wt) cycle only -Ve 211 Sign the 59 in uare 27 1/2 Im² coszwt) 2 d(wt) 27 12 $\frac{10t - sin 2wt}{2} \int_{0}^{2\hat{1}}$ Im² Ξ 417 1/2 Im² -411 Im 5 J2 4 m to. Im 097, 12 3)* 2IT pple factor Inms Im² Red = IDC ZI 2 - 1 × 4-1-2 Mr. T 4 Im² 1.21 TI2 2 Im 0.48 Downloaded from : uptukhabar.net

=) n= 0.48 9 and shall swamp inter (g it The preser greet and very 4) * Rectification Efficiency: - RECTIONAR THREE IN $\frac{9}{2}\eta = \frac{I_{DC}^{2} \times 100}{I_{AC}^{2}} = \frac{4Im^{2} \times 2 \times 100}{\Pi^{2}}$ $I_{MC}^{2} = \frac{1}{12} I_{MC}^{2}$ $= 0.81 \times 100 = 81^{\circ/\circ}$ $\Rightarrow [\eta = 0.8] \text{ on } [/.\eta = 81]/.$ 5) * Average on DC voltage: $V_{DC} = I_{DC} \times R_{L}$ - Anterente Desanifition - $= \frac{2 \operatorname{Im} \times R_{1}}{\pi}$ AA? MIN $= 2 \sqrt{m}$ $(R_L + R_S + R_F) \overline{n}$ = 2Vm providence ($\Rightarrow V_{DC} = 2V_{m}$ 6) * AC on RMS load voltage: $\frac{V_{mms} = I_{mms} \times R_l}{\sqrt{2}} = \frac{I_m \times R_l}{\sqrt{2}}$ Downloaded from : uptukhabar.net $= \delta V_m \qquad \times R_L = V_m$ $(R_L + R_S + R_F)\sqrt{2}$ $W = \sqrt{2}$ Actoria the Leasting of A wind - ve fellanthe win => N Vnms => Vm 2000 monga

Full wave Rectifien <u>* 2)</u> V.V.V.V. 8mp (ii) BRIDGE RECTIFIER :-DI 24 Ø 2 => Cincuit Description -It consists of a transformer and four diodes with 0 load nesistance It gives output for both cycles ø wonking \Rightarrow A Ðı D4 m D3 D2 Downloaded from : uptukha - B In +ve half cycle, the +ve polarity will appear • across the terminal A and -ve polarity will appear across the terminal B

In this cycle, the diade D, and Dz will become forward bias and Dz and Dy will become neverse bias. · The output across the load resistance 'R' will be in same phase with the input due to the diode D, and Oz as shown in figure. A-zin Weldage Anthiene est quademaken · In the -ve half cycle, the polarity gets reversed Jerminal A becomes -ve and B becomes +ve · In this cycle, D2 and D4 will be become forward bias and D, and D3 will be in neverse bias. · The output across the load resistance R' will be 180° outer phase with the input due to diode D2 and by, on with the same phase as the tre half cycle. => Input/output uaveform - de ange timeich de · Half wave unitage denition consists of two diddes and has capacitons along with the transformation ne sherry Downloaded from : uptukhabar.net

anna nr Vin 3N Π Input 2 Tî Vm 411 311 output 211 Π <u>Veltage Multiplier</u>: * Half wave Voltge Doubler 1) Full wave Voltage Doubler 2) Voltage Triplen on quadrapler adf genuit * 11) => HALF WAVE VOLTAGE DUBLER : TIT AT De E Vm AC) 2: Co ad while binauit Description - a march the first the good the ⇒ · Half wave voltage doubles consists of two diodes and two capacitors along with the transformer. as shown in the figure. Downloaded from : uptukhabar.net

=> Negative Half bycle -• During -ve half cycle, diede e, will be forward bias and er will be reversed bias. • In this cycle, capacitor c, will be charged through diode D, and it is given as, $-V_{m} + V_{G} = D$ $V_{c1} = V_{m}$ Positive flalf bycle During +ve half cycle, diode D2 will be forward bias and diode D, will be reverse biased. and an and a set of • The capacitor c_2 will be charged through diode D_2 , with the polarity of applied cycle. $V_m + V_{c1} - V_{c2} = 0$ aberb de vert - Ver + Ver metagoine $V_{c_2} = V_m + V_m$ $V_{c2} = 2 V_{m}$ · The output will be equal to Viz-* 12) = FULL WAVE VOLTAGE DOUBLER: · Auniary - Ve half anole Einne 181 with he enduranced bigs and D. will be to mand bigs Downloaded from : uptukhabar.net

21 2401 DZIEV =) consists of two diodes and two capacitons with a transformer. Positive Half bycle -⇒ During the half cycle, Diode d, will be forward - C1 bias diode D2 will be neversed bias and 0 Capaciton of will be changed through diode D, with the polarity of the cycle $V_m - V_{c1} = D$ Vers Vm then the Negative Half cycle= => -AARTIO During -ve half cycle, Diode D2 will be neversed 0 and Dz will be forward bias Capaciton C2 will be changed through diode D2 Downloaded from : uptukhabar.net

* For full wave voltage doubles view the circuit carefully and then understand. In -ve cycle hidden signs are Page No. there. Date with the polarity of -ve cycle willing - 62 $-V_{c_2} =$ Vcz = Vm Butput will be equal to - $V_0 = V_{c1} +$ Vo= Vm + Vm Vo = 2Vm * (3) > VOLTAGE RUADRUPLER JRIPLER DR Iniplen CI Дų \mathfrak{D}_3 DI C4 C2. Buddwillen Circuit Description -=) 15616 It consits of three diodes and three capacitors for Inipler along with a transformer and if for quadruplen then four diodes and four capacitors alongwith a transformer. Working -=> Downloaded from : uptukhabar net

1st Pasitive cycle - v planting the and the second $\frac{1}{\sqrt{1 + 0}} = \frac{1}{\sqrt{1 + 0}} = \frac{1}$ Vere Verent => The capaciton c, gets changed through diode D, and is given by -Vm - Vc1 = 0Ver=Vm - 1125 MANAL 6 (2) • 1st Negative cycle - $\begin{array}{c}
- & + \\
\uparrow & \vee c_{1} \\
\hline & \vee c_{1} \\
\hline & & & & & \\
\hline & & & & \\
\hline & & & & & \\
\hline \end{array} \\ \hline & & &$ => In finst -ve cycle, diede D, will become nevense bias (open circuit) and Dz becomes Sonward bias (short circuit). gt sensille of these diracs and there agan the > The capacitor & gets charged through diode Dozand his given by - 22 and wighthan $V_m - V_{C2} + V_{C1} = 0$ $V_m - V_{c2} + V_m = D$ $\Rightarrow V_{C_2} = 2V_m$ Downloaded from : uptukhabar.net

2nd positive cycle. Bergering midt ich G beaucal - 2450 Haraballa dates (Muraba Jerga) big + sheat distriction + Voi Vm-Dt-2Vm Vm ୬। D3 Ð2 Sell. -> REVENSE +1-1= Bias nord and they they they they they they Value = Vin + Value + Value lopen cincuit) > In this cycle, Di and Dz are in reverse bias and diede 23 becomes forward bias (short circuit). > The capacitor C3 gets charged through diode 23 and is given by -Vm - Vc1 - Vc3 + Vc2 = 0 Vc3 = Vm - Vc1 + Vc2 Ve3 = V/n - V/n + 2Vm = $V_{c3} = 2V_m$ JAT The output of the tripler is given by $V_0 = V_{C1} + V_{C3}$ $V_0 = V_m + 2V_m$ $V_0 = 3 Vm$ 2nd Negative cycle VCB 21 D3 22 24 Ym Vc2 ai vemit the Hiro Vcy Downloaded from : uptukhabar.net

=) In this cycle, D, De, D3 gets nevensed bias (open cincuit) and diade Dy gets forward bias (shont cincuit). => The capaciton Cy gets changed through diade Dy and is given by -Vm - Vc2 - Vc4 + Vc3 + Vc1 = D Vey = Vm + Vez - Vez + Vez (per cincic) bring and astraving the straver = Vm + Vm + 2Vm + 2Vm (finders funding) and i Vey = 2 Vm una ant & aback The output of the quadrupler is given by -Vo = Voz + Voy - marin of her $V_0 = 2V_m + 2V_m$ 2 Vo = 4 Vm 20V Mes E My my My to * ZENER DIDDE AS A SHUNT OR VOLTAGE REGULATOR 8-Is Rs e-vs-2 YIz YIm avitagan bre Vin Vz RL VL Izm -> max. value (always will be given) <u>Iz(min)</u> → D (always) Downloaded from : uptukhabar.net

ZENER DFODE AS A VOLTAGE REGULATOR

-> Voltage Regulator is a circuit whose function is to recontain a constant output Drc. actuge inspite of the Arc: exput variations or charge in load resultance values.

circuit Diagram

» A zener diode as a shart regulator circuit is shown in the figure

5 RS VIL 1 RL VL Regulated SKL VL Regulated Output 1I2

- => This is also known as shunt regulator because the Zener diode is connected in shunt or parallel with the load.
- => The Resistance Rs is also known as current limiter pessitor which is used to limit the current acress the zener diddle
- => The output or regulated caltage is obtained across the load resistor RL

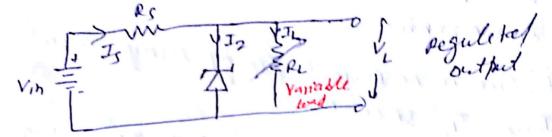
-> For the operation of the circuits the enpit valtage Vin Should be greater then zener diode voltage V2. Then only rener diode operates in breakdown region. => To find the input current, Apply KU is the Loop. => Vin = Isks + Vz Vs = Input die Unregulated valtage

=>] Is = Vin - Vz] V2 = Vallage across zener diode.

=> The eideal zener dicale may be assumed as a constant voltage source of voltage 1/2. => The load valtage is then given by MULTING VL = VZ => The current through the load pessistance is givening II = VL RL MAX NY MAN >> Applying KCL, the input current will be given by Is= IztIL => [Iz = Is-IL] working operation The working of voltage segulator is employmed in two Barts. Case I For variable enput Supply > In this Case, the load resistance Ris kept constant (fixed) and the inflict voltage (Win) is variand => color the inputvaltage increases, the input current Is also increases. Since Is = IztIL RS ERL VE regulated I Constant J Variable > This increased current 3, increases the current through the zener didle without affected the load > Due to increase in input airrent Is, the valtage dep across Resistence is also increases and keeping load with VI. Constant.

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> Now the relfage decreases, the input apprent also dereases one to the the current through rener diverse also decreases. > withose drop across serves resuspence is peducod, hence the load withoge VL and load current 32 reason constant. Caret: For load pesistence is vasiable input is filled > In this Case, the input vactage Vm is kept constant and the load pesistence to varied.



> The load resistance Re decreases, the load current increases This cause rener divele current to decrease, due to they inflid current Is & doop across the imput peristance remains Constant. Therefore the load valleage ve is also constant > How the load resistance Re, increases, the load current dercreases. Due to this rener current increase > This again keeps the values of expect current the vallage dup across suives resistance as constant. > Therefore, the load vallage remound constant.

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Determine the range of values of Vi that will main-Bues tain the zener diode in the DN state for the given cincuit. + IS 22052 1.2 K. J. EVS -> YIZ Vz=20V $\forall :$ IZM = 60 mA $Griven - V_Z = V_L = 20V , R_L = 1.2 K D.$ Soln $\frac{F_L}{F_L} = \frac{2D}{1.2 \times 10^{+3}} = 16.66 \times 10^{-3} \text{ A}$ Ille: todh it broad for and it articult Vi = Vs+ VLander Vi = Vs + Vz \Rightarrow $V_i = V_s + 2p - 0$ Vilmax) = Vs(max) + 20 - 2 $V_{i(min)} = V_{s(min)} + 20 - 3$ Dim - SV (= UI- 1- SV $I_{S} = I_{2} + I_{1} - O$ =) Is = Iz + 16.67 --- 5) = Istmax) = 60 + 16.67 = 76.67 mA T. T. T. T. Is(min) = 0+16.67 = 16.67 mA Pere the contract walk a subject to the star

 $\frac{-1}{10} = \frac{1}{10} \frac{1}{10} = \frac{1}{10} \frac{1}{$ require anti- may shop 176.6 11 × 12 20 at 201137 att read dimerio. = 36.8 6V Vilmin) = (16.67 × 10-3 × 220) + 20 - 15 - 23.66 V - 5V -1Kr And These Rues $\leftarrow v_s \rightarrow \psi I_z$ IL Vin=50V - Vz=10V-A ZARE VL Izm=10mA + JEX Determine the range of Ri and It that will result in V being maintained at 10 V. Given - Izimax) = 10 mA Son $V_Z = V_L = 10 V$ $V_{in} = V_S + V_Z$ $50 = V_{S} + 10 = V_{S} = 40V$ TH T $\frac{I_s = V_s = 40}{R} = \frac{40}{1 \times 10^3} = \frac{40 \text{ mA}}{R} = \frac{40 \text{ mA}}{1 \times 10^{+3}}$ Port T2 JE = Iz tite T2 = Connect $I_l = I_s - I_z$ Americal Iz = 40mA - Iz - 0 for the minimum value of IL => Iz should be maximum Downloaded from : uptukhabar.net

Maximum It then Iz should be minimum RL 1228153 IL(max)= 40 - 0 = 40 mA Tto I at Th $\frac{J_{l}(min) = 4D - 1D = 3DmA}{\overline{5}}$ VL = JL × RL SOLXI $\frac{2}{12} R_{L} = \frac{V_{L}}{I_{L}}$ R_L max, when I_L is minimum Rimin when I is max. $R_{L(max)} = 10 = 0.333 \text{ Kn}$ 30×10^{-3} $R_{L}(min) = \frac{10}{40 \times 10^{-3}} = 0.250 \text{ K.n.}$ $R_{s} = 1K \cdot n$ $(-v_{s} \rightarrow Y Iz \quad Y I_{L}$ Ques $\frac{V_{in} = 16V}{V_z = 10V}$ ZRL=1.2K-1. Find out V1, Vs, Iz and Pz (power across zenen diode). Soln $V_{in} = V_s + V_z$ 16 = VS + 10 \rightarrow Vs = 6V $\frac{V_{L}}{R_{L} + R_{S}} = \frac{1.2 \times 10^{3} \times 16}{1.2 \times 10^{3} + 1 \times 10^{2}} = \frac{8.72 \vee 10^{3}}{1.2 \times 10^{3}} = \frac{1.2 \times 10^{3} \times 16}{1.2 \times 10^{2}} = \frac{1.2 \times 10^{2}}{1.2 \times 10^{2}}$ Downloaded from : uptukhabar.net

= 7.27 mA 8.72 IL = YL Ē 1.2 × 10 3 RL = $I_2 + I_L$ Ic 6 <u>= 6m</u> Vs Rs 5 Ig = 1×103 $I_{S} = I_{Z} + I_{L}$ 7 = 6 - 7.27 $I_{Z} = I_{S} - I_{L}$ 2.2.2 - 22 Y 78 . $\mathbf{h}_{ij}^{(1)}$: ci= 1 J Flord 17 Downloaded from : uptukhabar.net 13

* Special Purpose Diode LED 1) BEFAREN LCD PUDUALAND Junnel Diede Varactor Diede 4) 5) Photo Digle 1) • LED (Light Emitting Diode): It is an optoelectronic device [which emits light] => It is an optical diode which emits light when it is ⇒ in forward biased. ⇒ Symbol of IED >> Construction of LED -ヨ * Holes Electrons P-type > Active Substrate > N-type The construction of LED is made up of depositing 0. semiconductor layer on the substrate. The active negion is between p-type and n-type 0 semiconductors Downloaded from : uptukhabar.net

· Electrons and holes recombine in active region and emits light. =) Basic operation -• When the p-n junction is forward bias, e-s cross the junction from n-type to p-type and recombine with holes. The similar operation is being taken place in LED diode. In LED diede, Grans (Grallium Ansenide) is used as a semi conductor material, in case of forward bias, the electrons and holes moves at active region where they recombine According to the property of GraAs, it emits light (invisible) while recombination · The free e's releases energy in the form of photons which emits light energy also called Electroluminescece In Silicon and germanium diode, the greater percentage of energy is converted in the form of heat during recombination, that's why, they are not used under construction of LED devices. Various impurities are added during doping process to control the wavelength of different colour of emitted light. [GIAN -> Blue, GIAP -> GIREEN, GIAASP -> Red on onange Downloaded from : uptukhabar.net

2) -> LCD (Liquid Crystal Display): It consists of thin layer of liquid crystal sandwiched between two glass sheets with thansparent electrodes. If both the glass sheets are transparent then it is called transmittive type cell. => If only one glass sheet is transparent and other have rejectling coating, the cell is called Reflective type cell. Sheet Electrodes Spacer or sealer Liquid Crystal => Jypes of Displays of LCD :-- (a) Field Effect 100 (b) Dynamic Scattening Display LCD S. S. C. [30x0 Downloaded from : uptukhabar.net

(a) 2	Field Effect ICD
	the second because the second bus
•	It consists of front and back polarisen at night
	angles to each other:
-	
•	Without electrical excitation, the light coming throu-
	gh the front polarisen is notated by 90° in the
	fluid and reflected back by the minnor
2	
	when electrostatic field is applied, liquid crystal
	molecules notate 90° so that light is not reflected and
	absorbed by the neal polarison. And, this nesults
	in dark digits on light background.
(b) 3	Dynamic Scattening Display 102:
0	when this display is energised, the molecules of
	energised area become turbulant and scatters
2	light in all the directions. And, this activated area
li •	results in silver display.
\rightarrow	Appications of LCO:
	Seven segment Display watches, portable instru- ments, television display.
	nvents, television display.
2)	
<u> </u>	Junnel Diode:
e	Men lunande d'a da la se tangente a series
	The tunnel diede is a two terminal pn-junction heavily dated about they sand linearly about them
	heavily doped about thousand times higher than
	a conventional diode & it has very flight
	conductivity.
Contraction of the second second	Downloaded from : uptukhabar.net

=) Due to treaving deping, the depletion layer width is reduced and because of de reduced depletion tayer carriers penetrate through ~ even when they don't possess enough energy to overcome the barrier. In mechanism of conduction in which charge carriers having very little energy penetrates a barrier instead of climbing over it is called Junneling. And, the didde constructed using this phenomenon is called Junnel Diode. ⇒ VI - characteristics of Junnel Diode : Frisi prinstant strenge er Peak Ip Negd-4 Hve Hve negistance V Negd-4 Hve negistance V Negd-4 Hve Negd-4 Hve Negd-4 Hve Negd-4 Hve Negd-4 Hve Negd-4 Hve Negd-4 Negd-4 Hve Negd-4 For small value of voltage, resistance remains 1. small and current attains a peak value 'Ip' corresponding to 'Vp'. 5) + Carrie a 2. At peak, dI = 0 where dI represents a slope. dV dV3.º Furthur, voltage increases current will decrease and dI becomes -ve and this -ve resistance dv Downloaded from : uptukhabar.net

4. Jurthur increasing the voltage, there will be exponential rise in current as in Page No. normal pn - junction diode. Date continue upto the value voltage 'Vy' corresponding to current 'I' and dI becomes D (zero) again Symbol of Junnel Diede : 衤 Ð Equivalent bincuit : Ls mm Rs y)• ⇒ varacton Diode :-In practice, a special type of diode is manufactured which shows the transistor capacitance property more predominantly as compared to conventional diode, is called <u>Varactor Diode</u> $C_T = \frac{n}{(v_J + v_R)^{\gamma_1}}$ Applications of Varactor Diode Juned circuit FM modulator Automatic Frequency controlled device Downloaded from : uptukhabar:net

5 Photo Diode

- . It is a spicial type of PN junction denice that generatis current when exposed to light is known as photodiode. It is also known as photodetector or photosensor. It operates in reverse brased mode and concerts light energy into electrical energy
- · symbol



hlorking

- · An the photodiode, a very small reverse current flow through device, that is termed as dark when It is when the device is not exposed to radiation.
- · when durice exposed to light, temperature of diode increases so the minority charge carriers increases. This generates high neverse interest
 - . This arrent shows that there is radiation or light on we can say that energy of light is diructly proportional to unrent through the duice.